XFP-AT-LP-51-80

10 Gb/s 80 km XFP Optical Transceiver

XFP Series

- **Hot-pluggable XFP footprint**
- **Supports 9.95 Gb/s to 11.3 Gb/s bit rates**
- **Supports lineside and XFI loopback**
- **RoHS-6 Compliant (lead-free)**
- **Power dissipation <3.0 W**
- **3.3 V & 1.8 V power supply**
- **Max. link length of 80 km**
- **Cooled 1550 nm EML and APD receiver**
- **Full duplex LC connector**
- **No reference clock required**
- **Built-in digital diagnostic functions**

ASCENT's XFP-AT-LP-51-80 Small Form Factor 10G (XFP) transceivers are designed for use in 10-Gigabit Ethernet links up to 80km over single mode fiber. It is widely used in applications such as Internet Service Provider (ISP) Fiber To The Home aggregation and backbone, Various Data Communication 10G Ethernet & SDH/SONET/OTN Links, Data Center networking for Ethernet and Fiber Channel SAN Networking and other optical links.

The module consists of 1550 EML Laser, InGaAs PIN and Preamplifier in a high-integrated optical sub-assembly. It is compliant with the current XFP Multi-Source Agreement (MSA) Specification. They comply with 10-Gigabit Ethernet 10GBASE-ZR/ZW per IEEE 802.3ae and 10G Fiber Channel 80KM.
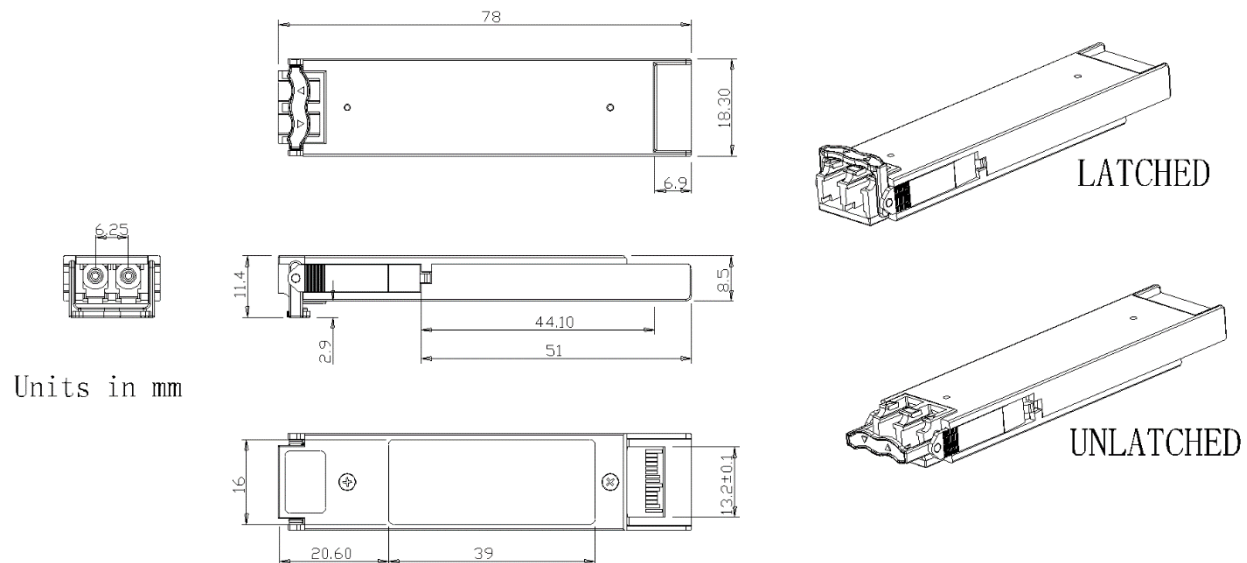
Digital diagnostics functions are available via a 2-wire serial interface, as specified in the XFP MSA. It also defines a sophisticated system of alarm and warning flags, which alerts end-users when particular operating parameters are outside of a factory set normal range.

The transceivers are RoHS compliant and lead free per Directive 2002/95/EC3.
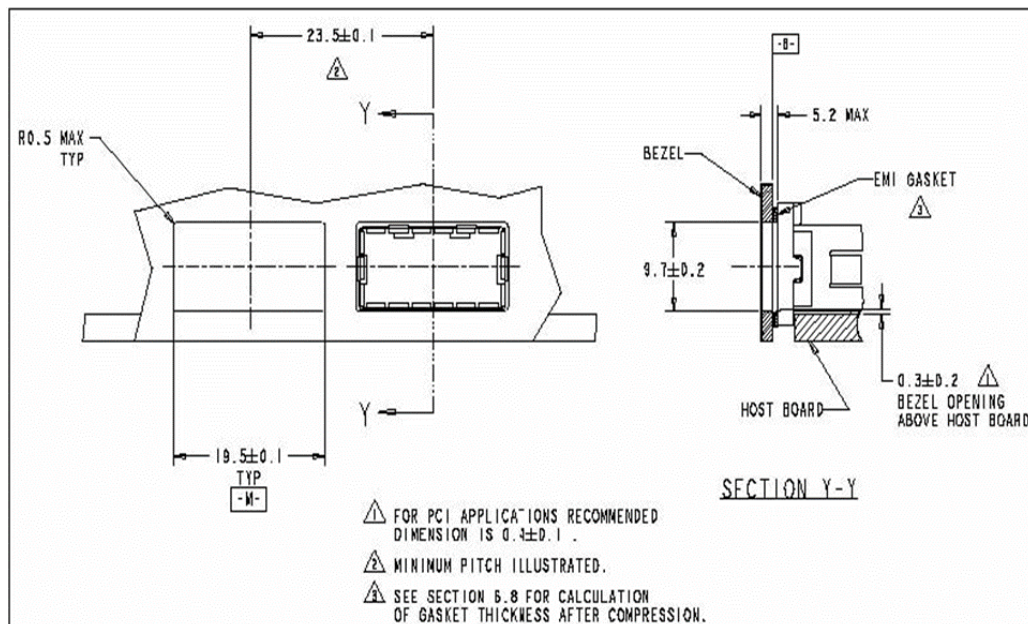
Key Features

- Hot-pluggable XFP footprint

- Supports 9.95 Gb/s to 11. 3Gb/s bit rates

- Supports Lineside and XFI loopback

- RoHS-6 Compliant (lead-free)

- Power dissipation <3.0 W

- 3.3 V & 1.8 V power supply

- Max. link length of 80 km

- Cooled 1550 nm EML and APD receiver

- Full duplex LC connector

- No reference clock required

- Built-in digital diagnostic functions

- Standard bail release mechanism

- Case operating temperature range: Commercial: 0°C to +70°C, Industrial: -40°C to +85°

Outline Diagram

XFP-AT-LP-51-80 Mechanical Specifications

PCB Layout and Bezel Recommendations

XFP Host Board Mechanical Layout (dimensions are in mm)

XFP Detail Host Board Mechanical Layout (dimensions are in mm)

XFP Recommended Bezel Design (dimensions are in mm)

Pin Assignment
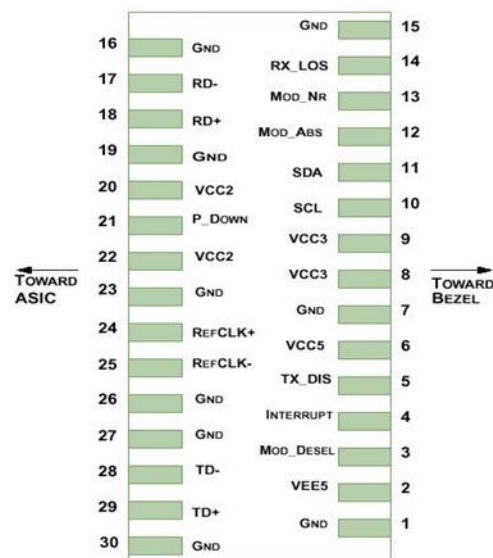
Diagram of Host Board Connector Block Pin Numbers and Name

Pin	Logic	Symbol	Name/Description	Note
1		GND	Module Ground	1
2		VEE5	Optional –5.2 Power Supply – Not required	

3	LVTTL-I	Mod-Desel	Module De-select; When held low allows the module to respond to 2-wire serial interface commands	
4	LVTTL-O	Interrupt	Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Transmitter laser source turned off	
6		VCC5	+5 Power Supply	
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I	SCL	Serial 2-wire interface clock	2
11	LVTTLI/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Module Absent; Indicates module is not present. Grounded in the module.	2
13	LVTTL-O	Mod_NR	Module Not Ready; ASCENT defines it as a logical OR between RX_LOS and Loss of Lock in TX/RX.	2
14	LVTTL-O	RX_LOS	Receiver Loss of Signal indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver inverted data output	
18	CML-O	RD+	Receiver non-inverted data output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply – Not required	
21	LVTTL-I	P_Down/RST	Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply – Not required	
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – Not required	3
25	PECL-I	RefCLK-	Reference Clock inverted input, AC coupled on the host board – Not required	3
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter inverted data input	
29	CML-I	TD+	Transmitter non-inverted data input	
30		GND	Module Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7 kΩ to 10 kΩ on host board to a voltage between 3.15 V and 3.6 V.
3. A Reference Clock input is not required by the XFP-AT-LP-51-80. If present, it will be ignored.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Maximum Supply Voltage 2	Vcc2	-0.3		3.6	V	
Maximum Supply Voltage 3	Vcc3	-0.3		2.0	V	
Storage Temperature	TS	-40		85	°C	
Case Operating Temperature	Tcase	0		70	°C	Commercial
		-40		85	°C	Industrial

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage – 1.8V supply	Vcc2	1.71		1.89	V	
Supply Voltage – 3.3V supply	Vcc3	3.13		3.47	V	
Supply Current – 1.8V supply	Icc2			250	mA	
Supply Current – 3.3V supply	Icc3			760	mA	
Module Total Power	P			3.0	W	1
Transmitter						
Input Differential Impedance	R_{in}		100		Ω	2
Differential Data Input Swing	$V_{in,pp}$	120		820	mV	
Transmit Disable Voltage	V_D	2.0		Vcc	V	3
Transmit Enable Voltage	V_{EN}	GND		GND+ 0.8	V	
Transmit Disable Assert Time				10	µs	
Receiver						
Differential Data Output Swing	$V_{out,pp}$	340	650	850	mV	4
LOS Fault	$V_{LOS\ fault}$	Vcc - 0.5		Vcc_{HOST}	V	5
LOS Normal	$V_{LOS\ norm}$	GND		GND+0.5	V	5

Notes:

1. Maximum total power value is specified across the full temperature and voltage range.
2. After internal AC coupling.
3. Or open circuit.
4. Into 100 Ω differential termination.
5. Loss Of Signal is an open collector to be pulled up with a 4.7 kΩ to 10 kΩ resistor to 3.15 V to 3.6V. Logic 0 indicates normal operation; logic 1 indicates no signal detected.

Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter						
Output Optical Power	Pf	0		5	dBm	
Optical Wavelength	λ	1530	1550	1570	nm	

Side mode Suppression Ratio	SMSR	30			dB
Optical Extinction Ratio	ER	8.2			dB
Avg. Launch Power of OFF Transmitter	POFF			-30	dBm
Eye Mask Margin		30			%
Receiver					
Receiver Sensitivity	R_{SEN}			-24	dBm 1
Input Saturation Power (Overload)	P_{sat}	-6			dBm
Wavelength Range	λ_C	1270	1610		nm
Receiver Reflectance	R_{rx}			-27	dB
LOS De-Assert	LOSD			-27	dBm
LOS Assert	LOSA	-37			dBm
LOS Hysteresis		0.5			dB

Notes:

1. Measured with BER < 10^{-12} @ 10.3 Gbps, 2^{31}- 1 PRBS.

Regulatory Compliance

Feature	Reference	Performance
Electrostatic Discharge (ESD)	IEC/EN 61000-4-2	Compatible with standards
Electromagnetic Interference (EMI)	FCC Part 15 Class B EN 55022 Class B (CISPR 22A)	Compatible with standards
Laser Eye Safety	FDA 21CFR 1040.10, 1040.11 IEC/EN 60825-1, 2	Class 1 laser product
Component Recognition	IEC/EN 60950, UL	Compatible with standards
ROHS	2002/95/EC	Compatible with standards
EMC	EN61000-3	Compatible with standards

Digital Diagnostic Functions

As defined by the XFP MSA, ASCENT XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the XFP MSA Specification.

Ordering Information

Product name	Product description
XFP-AT-LP-51-80	XFP Plug-in, 10 Gbps, 80 km, TX=1550/RX wide, on two single mode fibers, LC/PC Blue
XFP-AT-LP-51-80A	XFP Plug-in, 10 Gbps, 80 km, TX=1550/RX wide, on two single mode fibers, LC/PC Blue, Industrial Temp

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