400 Gb/s QSFP-DD LR4 10 km Transceiver

QSFP-DD Series

- Compliant to QSFP-DD MSA
- 4 CWDM lanes
- 100G Lambda MSA 400G-LR4 compliant
- Duplex LC connector
- Up to 10 km transmission range over SMF with FEC
- Up to 106.25 Gbps (PAM4) per channel
- RoHS compliant

Ascent's QSFP-DD-LP-10 is a 400 Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) optical module designed for 10km optical communication applications. The module converts 8 channels of 50 Gb/s (PAM4) electrical input data to 4 channels of CWDM optical signals, and multiplexes them into a single channel for 400 Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 400 Gb/s optical input into 4 channels of CWDM optical signals, and converts them to 8 channels of 50 Gb/s (PAM4) electrical output data.

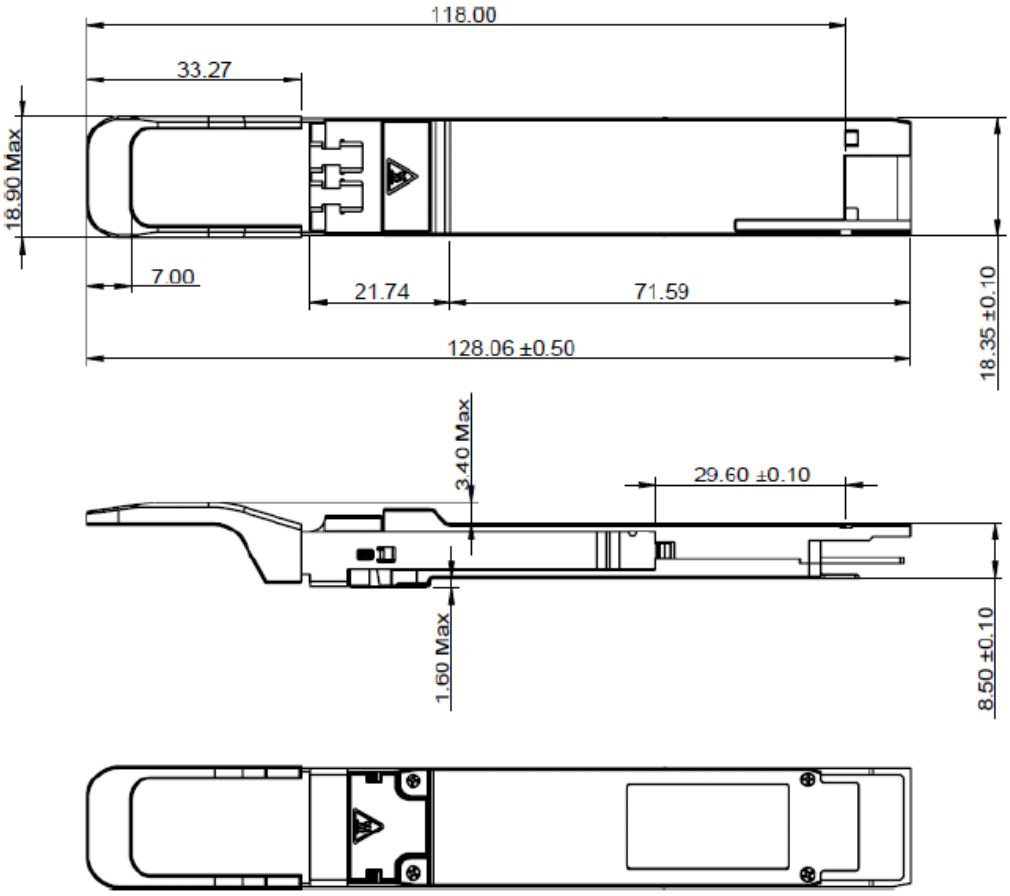
The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains a duplex LC connector for the optical interface and a 76-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module. Host FEC is required to support up to 10 km fiber transmissions.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Multi- Source Agreement (MSA) Type 2. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

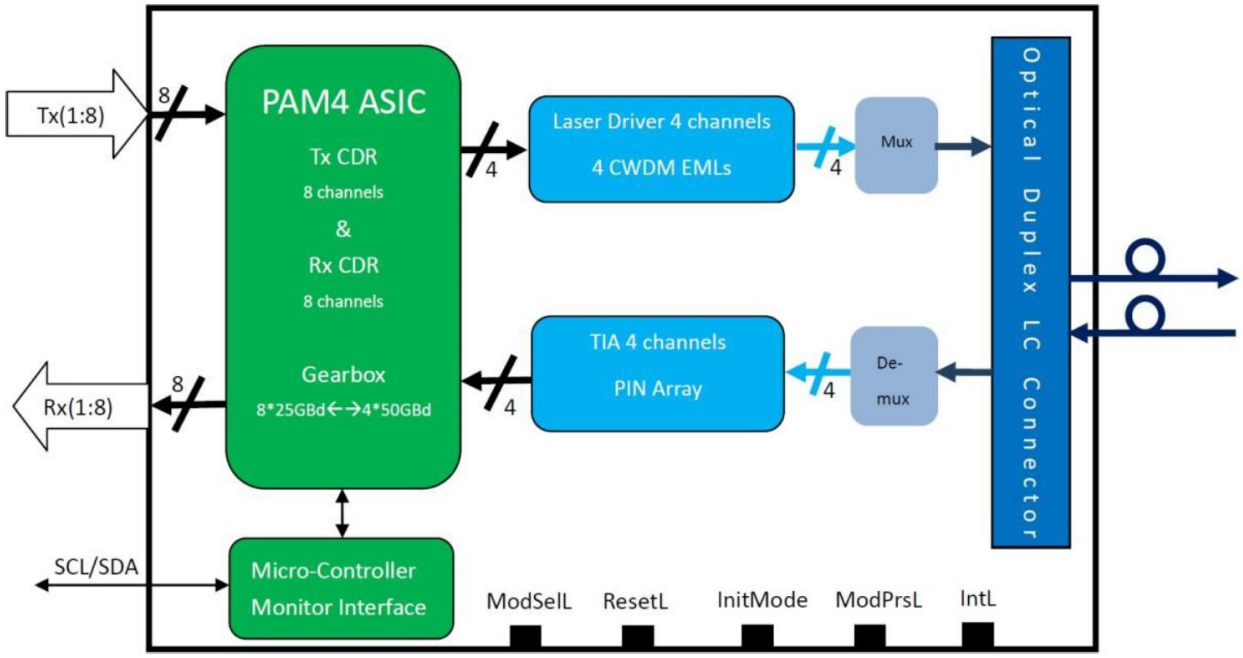
Key Features

- Compliant to QSFP-DD MSA
- 4 CWDM lanes MUX/DEMUX design
- 100G Lambda MSA 400G-LR4 specification compliant
- Duplex LC connector
- Up to 10 km transmission distance on single-mode fiber (SMF) with FEC
- 8 × 53.125 Gb/s electrical interface (400GAUI-8)
- 106.25 Gbps (PAM4) data rate per channel
- Case temperature range: 0 °C to +70 °C
- Max. power consumption 12 W
- RoHS compliant

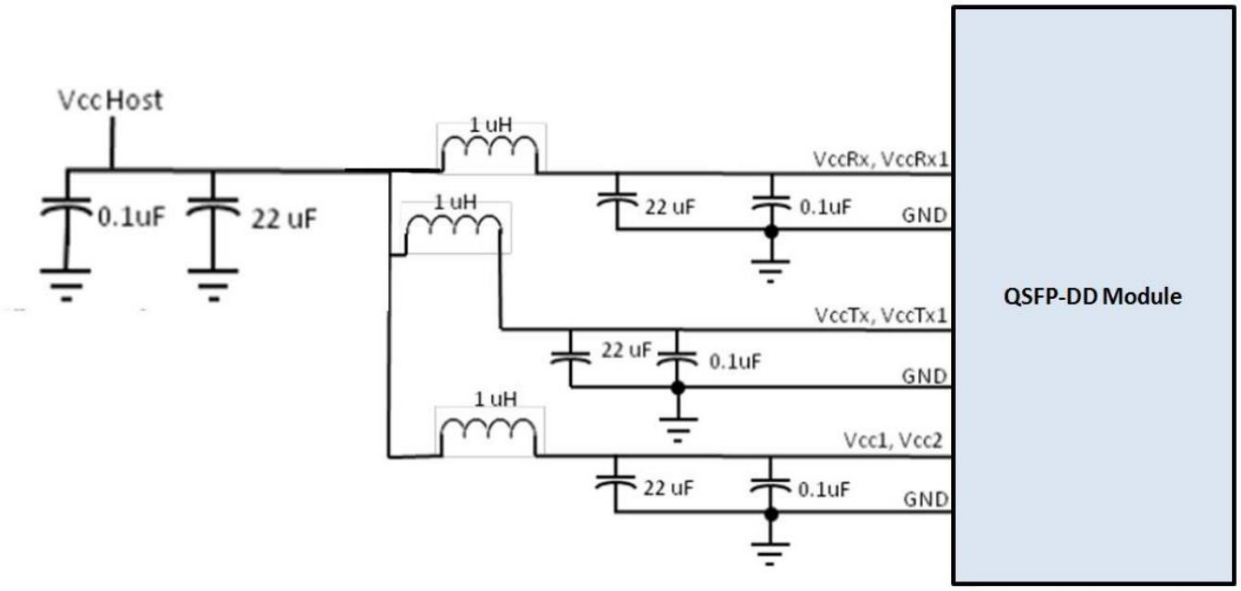
Outline Dimensions



Host-Transceiver Interface Block Diagram



Recommended Power Supply Filter



Functional Description

The module incorporates 4 independent channels on CWDM4 1271/1291/1311/1331 nm center wavelength, operating at 1OOG per channel. The transmitter path incorporates a quad channel EML driver and EML lasers together with an optical multiplexer. On the receiver path, an optical de-multiplexer is coupled to a 4-channel photodiode array. A DSP basis gearbox is used to convert 8 channels of 25GBaud PAM4 signals into 4 channels of 50GBaud PAM4 signals and also an 8channel re-timer and FEC block are integrated in this DSP. The electrical interface is compliant with IEEE 802.3bs and QSFP-DD MSA in the transmitting and receiving directions, and the optical interface is compliant to IEEE 802.3bs with duplex LC connector.

A single +3.3V power supply is required to power up this product. All the power supply pins are internally connected and should be applied concurrently. As per MSA specifications the module offers seven low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, lnitMode, ModPrsL and Intl.

Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus - individual ModSell lines must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the memory map.

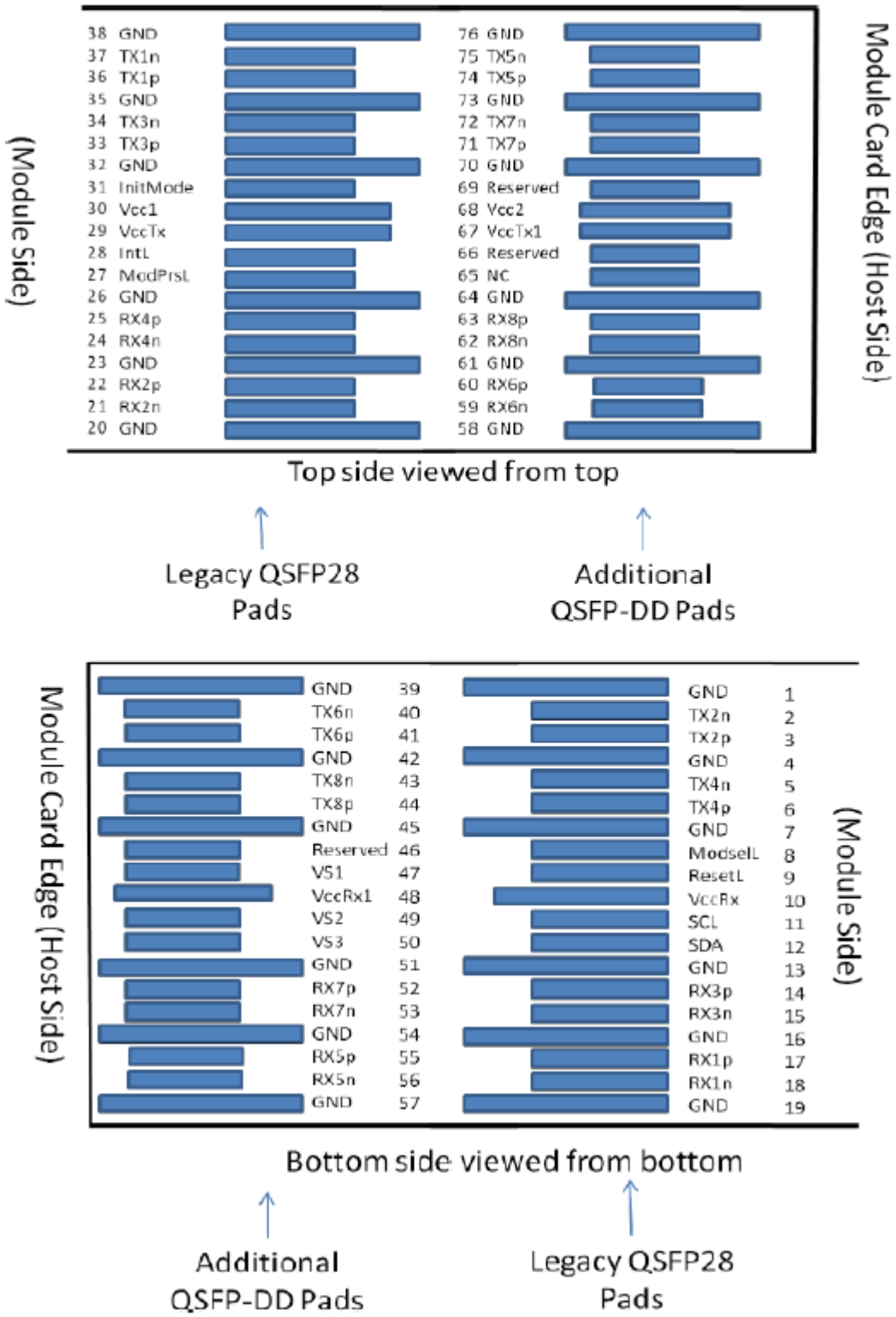
The Resetl pin enables a complete reset, returning the settings to their default state, when a low level on the Resetl pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an Intl (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Initialize Mode (lnitMode) is an input signal. It is pulled up to Vee in the QSFP-DD module. The lnitMode signal allows the host to define whether the QSFP-DD module will initialize under host software control (lnitMode asserted High) or module hardware control (lnitMode de-asserted Low). Under host software control, the module shall remain in Low Power Mode until software enables the transition to High Power Mode, as defined in the QSFP-DD Management Interface Specification. Under hardware control (lnitMode de-asserted Low), the module may immediately transition to High Power Mode after the management interface is initialized. The host shall not change the state of this signal while the module is present. In legacy QSFP applications, this signal is named LPMode. See SFF-8679 for LPMode signal description.

Module Present (ModPRsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates it's present by setting ModPrsL to a "Low" state.

Interrupt (IntL) is an output pin. "Low" indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the host Vcc voltage on the host board.

Pin Assignment



Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3 V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3 V Power Supply Transmitter	2B	2
30		Vcc1	+3.3 V Power Supply	2B	2
31	LVTTL-I	InitMode	Initialization Mode; in Legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Non-Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Output	3A	

42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Non-Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Output	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3 V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3 V Power Supply	2A	2
68		Vcc2	3.3 V Power Supply	2A	2
69		Reserved	For future use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Output	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Output	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Output	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Output	3A	
76		GND	Ground	1A	1

Notes:

1. QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, VccRxl, Vccl, Vcc2, VccTx and VccTxl shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTxl may be internally connected within the module in any combination. The connector Vee pins are each rated for a maximum current of 1000 mA.

3. All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kΩ and less than 100 pF.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1 B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

Specifications

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T_S	-40		+85	°C	
Operating Case Temperature	T_{OP}	0		+70	°C	
Relative Humidity	RH	0		85	%	
Power Supply Voltage	V_{CC}	-0.5		3.6	V	
Damage threshold, Each Lane	THd	5.0			dBm	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Operating Case Temperature	T_{OP}	0	-	+70	°C	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, Each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				2.4×10^{-4}		
Post-FEC Bit Error Ratio				1×10^{-12}		1
Transmission Distance	D	0.002		10	km	2

Notes

1. FEC Provided by host system.
2. FEC required on host system to support maximum distance

Optical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Wavelength Assignment	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Transmitter						
Modulation Format			PAM4			
Data Rate, Each Lane			53.125 ± 100 ppm		GBd	

Side-Mode Suppression Ratio	SMSR	30		dB	
Total Average Launch Power	P_T		10.0	dBm	
Average Launch Power Each Lane		-2.8		dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), Each Lane	P_{AVG}	0.2	4.2	dBm	2
Launch Power in OMA_{outer} - TDECQ, Each Lane	P_{OMA}	-1.2		dB	ER ≥ 4.5 dB
	P_{OMA}	-1.1		dB	ER < 4.5 dB
Transmitter and Dispersion Eye Closure for PAM4, Each Lane	TDECQ		3.9	dB	
TDECQ – 10*$\log_{10}$(Ceq), each lane			3.9	dB	3
Extinction Ratio	ER	3.5		dB	
Difference in Launch Power between any Two Lanes (OMA_{outer})			4	dB	
$RIN_{15.6}OMA$	RIN		-136	dB/Hz	
Optical Return Loss Tolerance	TOL		15.6	dB	
Transmitter Reflectance	R_T		-26	dB	
Transmitter Transition Time			17	ps	
Average Launch Power of OFF Transmitter, Each Lane	P_{off}		-20	dBm	
Receiver					
Modulation Format			PAM4		
Data Rate, Each Lane			53.125 ± 100 ppm	GBd	
Damage Threshold, Each Lane	TH_d	5.0		dBm	4
Average Receive Power, Each Lane		-9.1	4.0	dBm	5
Receive Power (OMA_{outer}), Each Lane			4.2	dB	
Difference in Launch Power between any Two Lanes (OMA_{outer})			4.6	dBm	
Receiver Sensitivity (OMA_{outer}), Each Lane	SEN		Equation (1)	dBm	6
Stressed Receiver Sensitivity (OMA_{outer}), Each Lane	SRS		-4.1	dBm	7
Receiver Reflectance	R_R		-26	dB	
LOS De-Assert	LOSD	-20		dBm	
LOS Assert	LOSA		-12.1	dBm	
LOS Hysteresis	LOSH	0.5		dB	
Stressed Conditions for Stress Receiver Sensitivity (Note 8)					
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			3.9	dB	
SECQ – 10 * $\log_{10}$(Ceq), Lane under Test			3.9	dB	
OMA_{outer} of each Aggressor Lane			0.5	dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

2. Even if the TDECQ < 1.4 dB for an extinction ratio of 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of <4.5 dB, the OMA_{outer} (min) must exceed the minimum value specified here.

3. C_{eq} is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for reference equalizer noise enhancement.

4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

5.The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.

6.Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.9dB. It should meet Equation (1), which is illustrated in the Illustration of Receiver Sensitivity Mask for 400G-LR4 seen below.

Equation 1: RS = max(-6.6, SECQ - 8.0) dBm

Where:

RS is the receiver sensitivity, and

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.

7. Measured with conformance test signal at TP3 for the BER equal to 2.4×10^{-4}.

8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

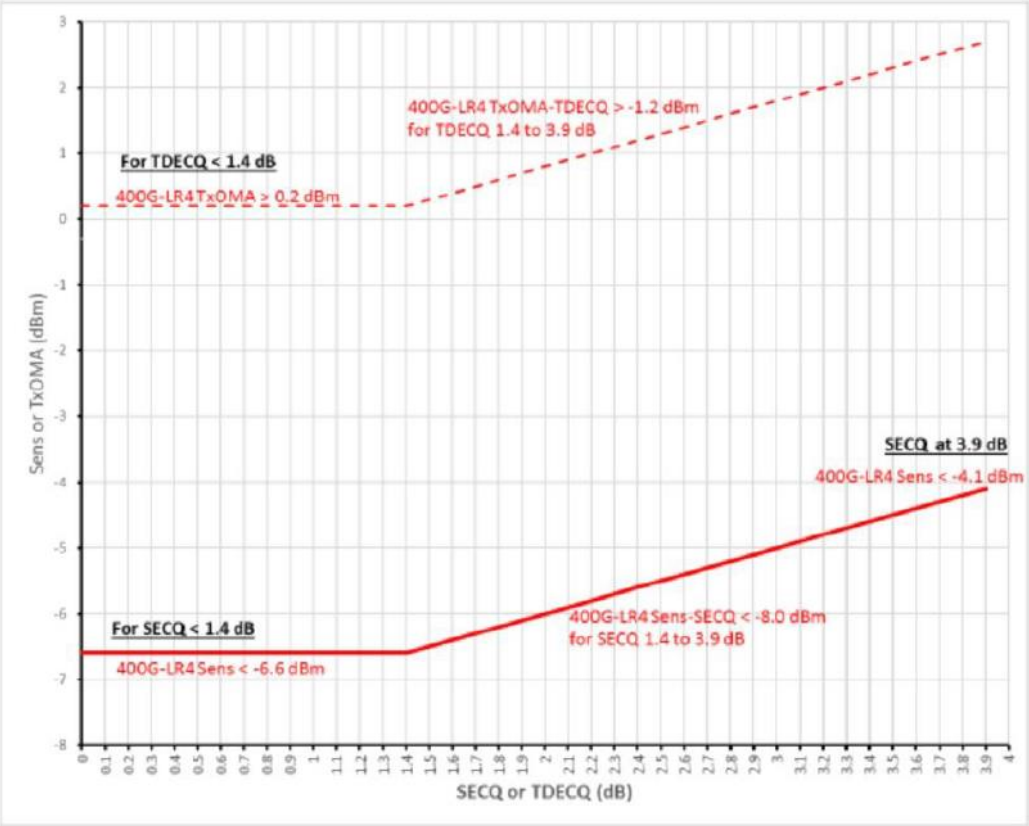


Illustration of Receiver Sensitivity Mask for 400G-LR4

Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Power Consumption				12	W	
Supply Current	Icc			3.64	A	
Transmitter (Each Lane)						
Signaling Rate, Each Lane	TP1		26.5625 ± 100 ppm		GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-Ended Voltage Tolerance Range (Min.)	TP1a		-0.4 to 3.3		V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	3
Receiver (Each Lane)						
Signaling Rate, Each Lane	TP4		26.5625 ± 100 ppm		GBd	
Differential pk-pk Output Voltage	TP4			900	mVpp	
AC Common Mode Output Voltage	TP4			17.5	mV	
AC Common Mode Output Voltage, RMS	TP4			10	%	
Differential Termination Mismatch	TP4	IEEE 802.3-2015 Equation (83E-2)				
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20 % to 80 %	TP4	9.5			ps	
Near-End Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-End Eye Height, Differential	TP4	70			mV	
Far-End Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-End Eye Height, Differential	TP4	30			mV	
Far-End Pre-Cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Digital Diagnostic Monitoring Information

Parameter	Symbol	Min	Max	Unit	Notes
Temperature Monitor Absolute Error	DMI_Temp	-3	3	°C	Over operating temperature range
Supply Voltage Monitor Absolute Error	DMI_VCC	-0.1	0.1	V	Over full operating range
Channel RX Power Monitor Absolute Error	DMI_RX_Ch	-2	2	dB	1
Channel Bias Current Monitor	DMI_Ibias_Ch	-10 %	10 %	mA	
Channel TX Power Monitor Absolute Error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single-mode fibers, there could be an additional ±1 dB fluctuation, or a ±3 dB total accuracy.

ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2 kV for all other electrical input pins, tested per MIL- STD-883, Method 3015.4/JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to EN 60825-1 :2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering Information

Product Name	Product Description
QSFP-DD-LP-10	QSFP DD PAM4 Plug-in, 400GBASE-LR4 10km, 1271, 1291, 1311 and 1331nm Optical Transceiver, LC Duplex, DOM

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