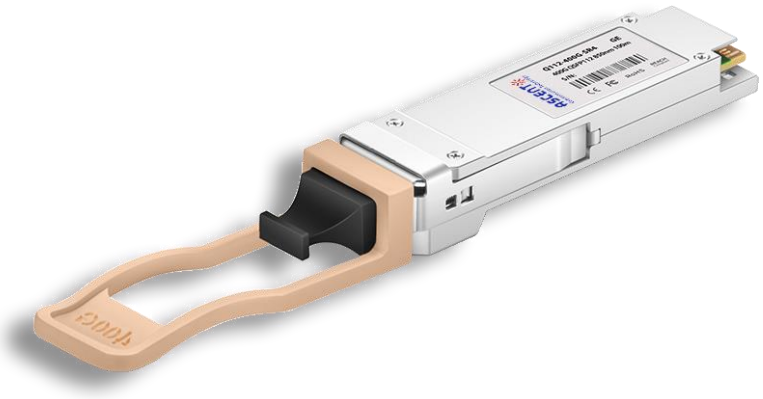
400G QSFP112 SR4 100 m Transceiver

QSFP112 Series



- 4x100G PAM4 retimed 400GAUI-4 electrical interface
- MPO-12 APC connector
- 4 channel VCSEL arrays
- 4 channels PIN photo detector arrays
- Maximum link length of 60 m on OM3 or 100 m on OM4
- Hot-pluggable QSFP112 form factor
- Compliant with QSFP112 MSA
- Compliant with CMIS 5.2
- Compliant with IEEE 802.3db
- Compliant with IEEE 802.3ck

Ascent's 400 Gbps QSFP112 SR4 transceiver is suitable for 400G ethernet and data center interconnect applications. It supports link lengths of up to 100m over MMF with MTP/MPO-12 connector. This transceiver is compliant with QSFP112 MSA, CMIS 4.0 Interface and 400GAUI-4 standards.

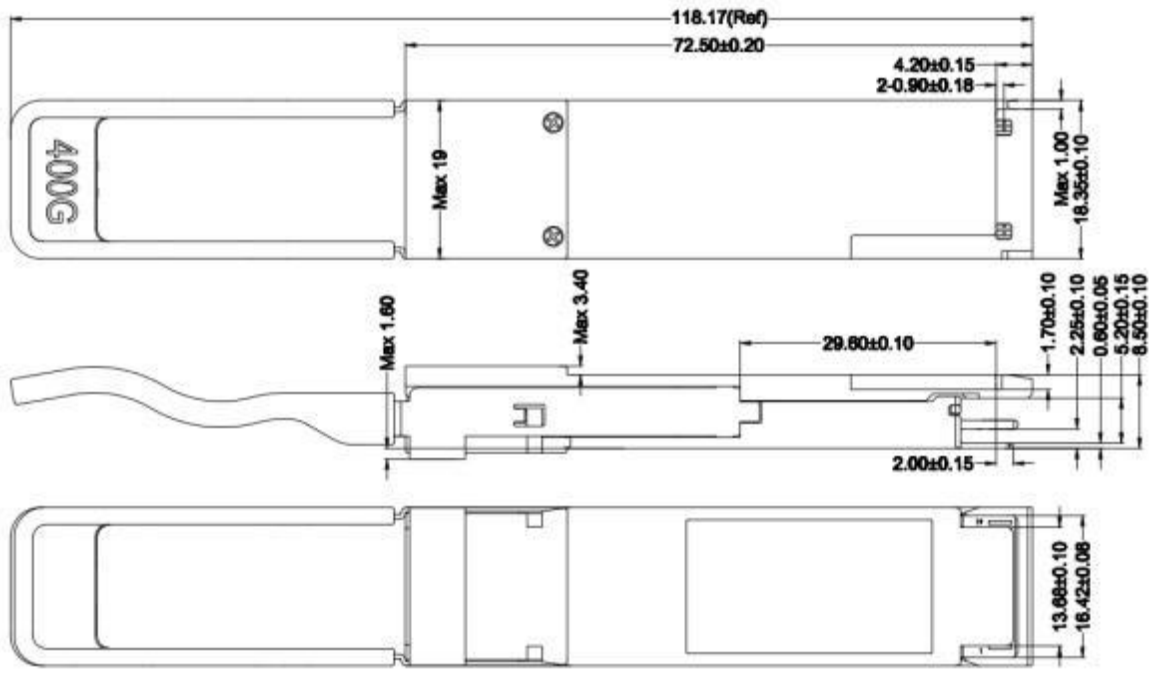
The 400 Gbps QSFP112 is a four-channel, parallel, pluggable, fiber-optic QSFP112 transceiver for 400 gigabit Ethernet applications. This transceiver is a high-performance module for short-range data communication and interconnects applications. It integrates four data lanes in each direction with 4x 53.125 GBd channels. The length of QSFP112 SR4 is up to 60 meters over OM3 MMF or 100 meters over OM4 MMF.

This module is designed to operate over multimode fiber systems using a nominal wavelength of 850 nm. The built-in digital diagnostics monitoring (DDM) allows access to real-time operating parameters.

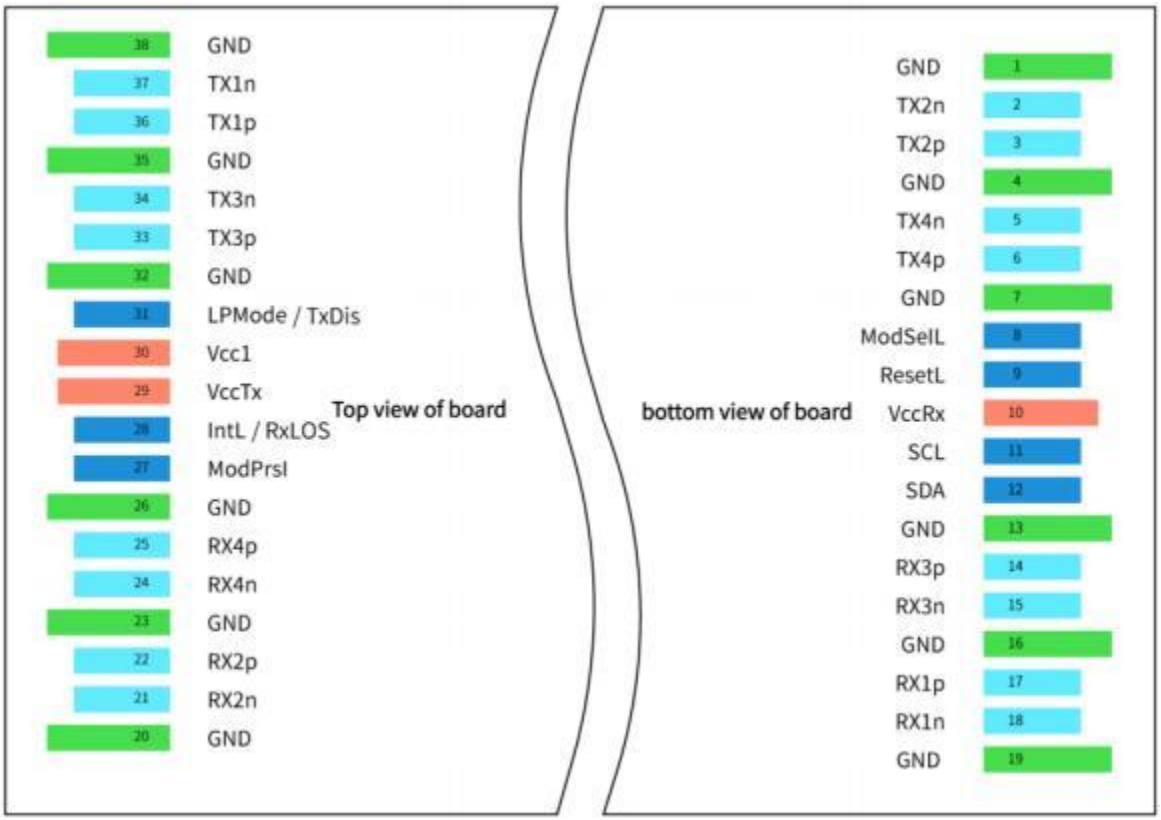
Key Features

- 4x100G PAM4 retimed 400GAUI-4 electrical interface
- MPO-12 APC connector
- 4 channel VCSEL arrays and 4 channels PIN photo detector arrays
- Maximum link length of 60 m on OM3 or 100 m on OM4
- Hot-pluggable QSFP112 form factor
- Compliant with QSFP112_MSA_Specification_Rev2.1.1
- Compliant with CMIS 5.2
- Compliant with IEEE 802.3db
- Compliant with IEEE 802.3ck
- Less than 8W in temperature range of 0 to 70°C

Outline Diagram



Pin Assignment



Pin	Name	Logic	Description	Power Sequence	Note
1	Ground		GND	1B	1
2	Tx2n	CML-I	Transmitter Inverted Data Input	3B	
3	Tx2p	CML-I	Transmitter Non-Inverted Data Input	3B	
4	Ground		GND	1B	1
5	Tx4	CML-I	Transmitter Inverted Data Input	3B	
6	Tx4p	CML-I	Transmitter Non-Inverted Data Input	3B	
7	Ground		GND	1B	1
8	ModSel	LVTTL-I	Module Select	3B	
9	ResetL	LVTTL-I	Module Reset	3B	
10	VccRx		+3.3V Power Supply Receiver	2B	2
11	SCL	LVCMOS- I/O	2-wire serial interface clock	3B	
12	SDA	LVCMOS- I/O	2-wire serial interface data	3B	
13	Ground		GND	1B	1
14	Rx3p	CML-O	Receiver Non-Inverted Data Output	3B	
15	Rx3n	CML-O	Receiver Inverted Data Output	3B	
16	Ground		GND	1B	1
17	Rx1p	CML-O	Receiver Non-Inverted Data Output	3B	
18	Rx1n	CML-O	Receiver Inverted Data Output	3B	
19	Ground		GND	1B	1

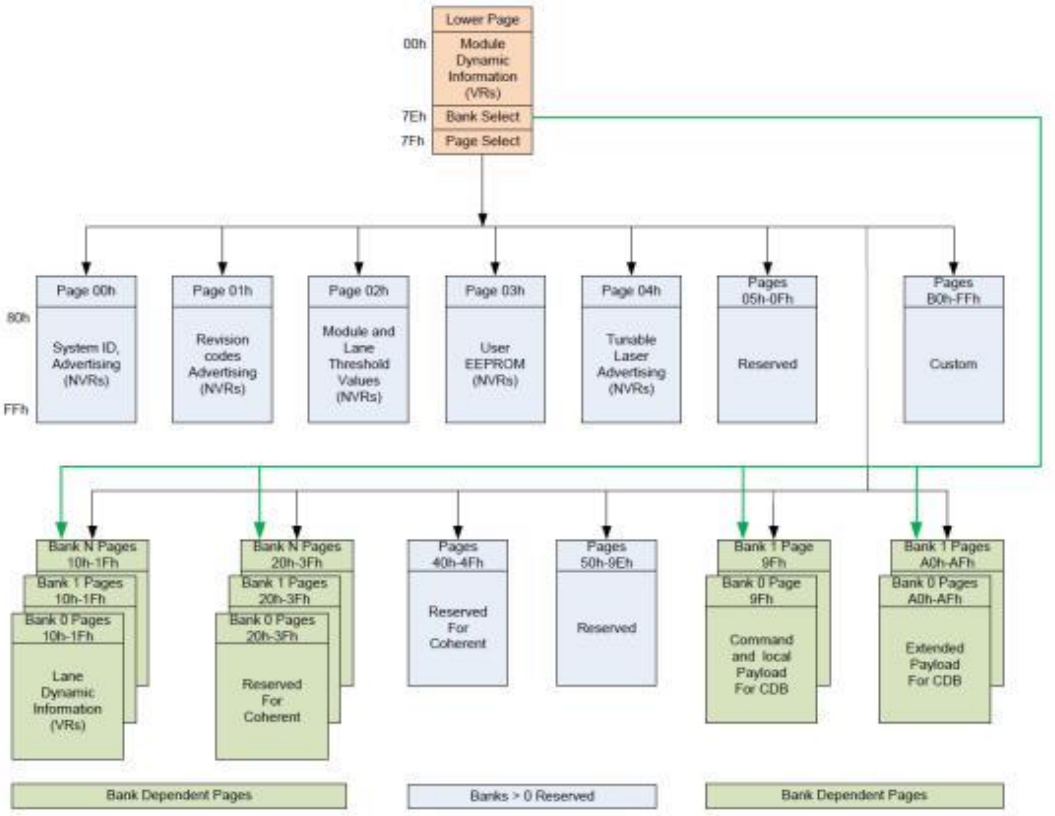
20	Ground		GND	1B	1
21	Rx2n	CML-O	Receiver Inverted Data Output	3B	
22	Rx2p	CML-O	Receiver Non-Inverted Data Output	3B	
23	Ground		GND	1B	1
24	Rx4n	CML-O	Receiver Inverted Data Output	3B	
25	Rx4	CML-O	Receiver Non-Inverted Data Output	3B	
26	Ground		GND	1B	1
27	ModPrsL	LVTTL-O	Module Present	3B	
28	IntL	LVTTL-O	Interrupt	3B	
29	VccTx		+3.3V Power supply transmitter	2B	2
30	Vcc1		+3.3V Power supply	2B	2
31	LPMode	LVTTL-I	Low Power mode	3B	
32	Ground		GND	1B	1
33	Tx3p	CML-I	Transmitter Non-Inverted Data Input	3B	
34	Tx3n	CML-I	Transmitter Inverted Data Input	3B	
35	Ground		GND	1B	1
36	Tx1p	CML-I	Transmitter Non-Inverted Data Input	3B	
37	Tx1n	CML-I	Transmitter Inverted Data Input	3B	
38	Ground		GND	1B	1

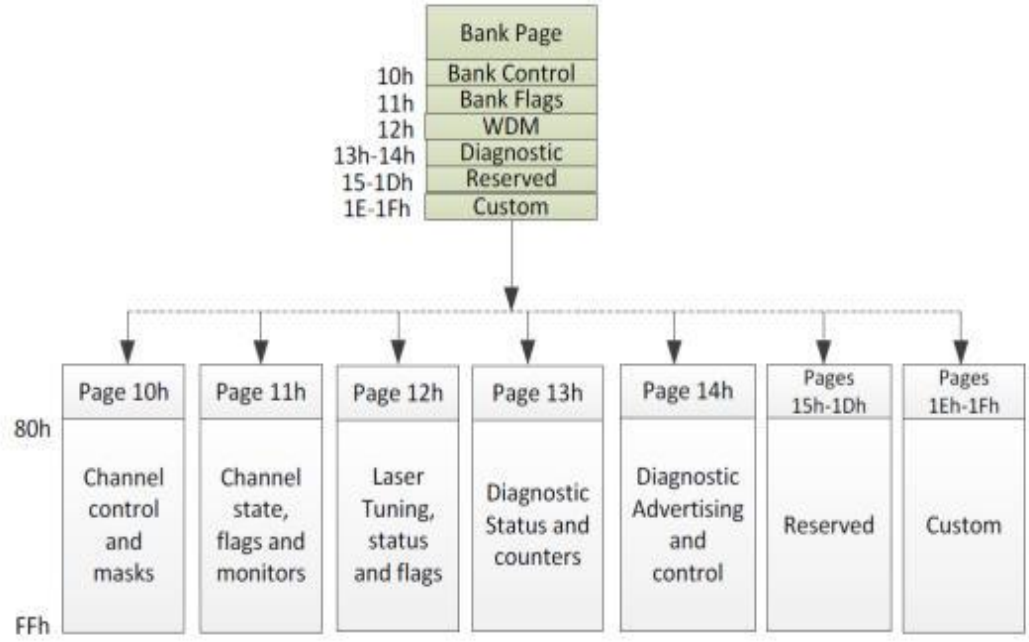
Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2. Vcc Rx, Vcc1 and VccTx are the receiver and transmitter power supplies and shall be applied concurrently. VccRx, Vcc1 and VccTx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5 A (max. current of 2.0 A is required for high module power of 15 W to 20 W).

Management Interface





Multiple Applications Support

400G QSFP112 SR4 supports CMIS 5.2 defined Application Advertising, Application Selection and Instantiation.

Application Advertising

Address (Dec)	Application AppSel Code	Name	Value (Hex)	Description
85	NA	Module Type encoding	1	Optical Interfaces: MMF
86	0001b	HostInterfaceID	4B	HostInterfaceIDApp1:100GAUI-1-S C2M
87		MediaInterfaceID	D	MediaInterfaceIDApp1:100GBASE-SR1
88		HostLaneCount&MediaLaneCount	11	LaneCountApp1:TX & RX 1 lanes
89		HostLaneAssignmentOptions	F	Permissible first host lane number: lanes 1, 2, 3, 4
01h:176		MediaLaneAssignmentOptions	F	Permissible first media lane number: lanes 1, 2, 3, 4
90	0010b	HostInterfaceID	F	HostInterfaceIDApp2:200GAUI-4
91		MediaInterfaceID	E	MediaInterfaceIDApp2:200GBASE-SR4
92		HostLaneCount&MediaLaneCount	44	LaneCountApp2: TX & RX 4lanes
93		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:177		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
94	0011b	HostInterfaceID	C	HostInterfaceIDApp3:100GAUI-4 C2M
95		MediaInterfaceID	0	MediaInterfaceIDApp3:100GBASE-SR4(SFF-8024 Undefined)
96		HostLaneCount&MediaLaneCount	44	LaneCountApp3: TX & RX 4 lanes
97		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:178		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
98	0100b	HostInterfaceID	4F	HostInterfaceIDApp4:400GAUI-4-S C2M
99		MediaInterfaceID	11	MediaInterfaceIDApp4:400GBASE-SR4
100		HostLaneCount&MediaLaneCount	44	LaneCountApp4: TX & RX 4 lanes
101		HostLaneAssignmentOptions	1	HostLaneAssignmentOptionsApp4: begin lane 1
01h:179		MediaLaneAssignmentOptions	1	Permissible first media lane number: lanes 1
102	0101b	HostInterfaceID	4D	HostInterfaceIDApp5:200GAUI-2-S C2M
103		MediaInterfaceID	1B	MediaInterfaceIDApp5:200GBASE-SR2
104		HostLaneCount&MediaLaneCount	22	LaneCountApp5: TX & RX 2 lanes
105		HostLaneAssignmentOptions	5	Permissible first host lane number: lanes 1, 3
01h:180		MediaLaneAssignmentOptions	5	Permissible first media lane number: lanes 1, 3
106			FF	HostInterfaceIDApp6:
107			0	MediaInterfaceIDApp6
108			0	LaneCountApp6
109			0	Permissible first host lane number

110	0	HostInterfaceIDApp7
111	0	MediaInterfaceIDApp7
112	0	LaneCountApp7
113	0	HostLaneAssignmentOptionsApp7
114	0	HostInterfaceIDApp8
115	0	MediaInterfaceIDApp8
116	0	LaneCountApp8
117	0	HostLaneAssignmentOptionsApp8

As shown in the table above, the Q112-400G-SR4-01 supports 5 applications, 400GBASE-SR4, 200GBASE-SR4, 100GBASE-SR4, 2X200GBASE-SR2 and 4X100GBASE-SR1

Application Selection and Instantiation

The host can select Applications by programming the AppSel value in Staged Set 0. AppSel=1 is the default Application populated in the Active Control Set at power-on or reset.

*Note that the channels of the module are independent and can be configured separately. (ie. up to four 100GBASE-SR instances can be configured), however, it does not support different applications with different channels at the same time.

Q112-400G-SR4-01 supports two methods of application selection and instantiation. The first method is implemented according to CMIS, and the second method is customized, which is simpler.

First method:

The applications switching configuration sequence is as follows: read Application Descriptor Registers and select the required Appel. Write application configuration to DPConfigLane<I>in Stage Control Set 0, then write 1 to ApplyDPInitLane<i> to trigger Application Instantiation.

The Active Set can be read from page 11 h.

For example, select AppDescriptor3:

Step 1: Write 0x30 in Page10h Byte145 to Byte152(8 bytes)—Set AppselCode3

Step 2: Write 0x00 in Page10h Byte143—Clear trigger register.

Step 3: Write 0xFF in Page10h Byte143—Set trigger register to run Application Instantiation.

Second method:

Set the value of Page10h Byte240. This is a private definition.

Code Value	Bit Pattern	Host Electrical Interface	Media Interface
0	00000000b	100GAUI-1-S C2M	100GBASE-SR1
1	00000001b	200GAUI-4	200GBASE-SR4
2	00000010b	100GAUI-4	100GBASE-SR4
3	00000011b	400GAUI-4-S C2M	400GBASE-SR4
4	00000100b	200GAUI-2-S C2M	200GBASE-SR2

TX & RX Squelch

Default TX and RX auto-squelch is enabled. But TX and RX auto squelch disable, and force squelching function are not supported

TX input equalization

Default TX adaptive equalization is enabled. But TX adaptive equalization disable, and fixed equalization adjust function are not supported.

RX output Equalization

RX output Equalization follows CMIS Table 6-7, with default 1dB, readable and writable.

Table 6-7 Rx Output Equalization Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	**Reserved**	**Reserved**
11-15	1011b-1111b	Custom	Custom

RX output amplitude

RX output amplitude follows CMIS Table 6-8, Rx output amplitude is the difference peak-to- peak EYE high when Rx output equalization is set to 0dB. The default value of output amplitude is set to 2, with typical differential 600mVp-p.

Table 6-8 Rx Output Amplitude Codes

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)
4-14	0100b-1110b	**Reserved**
15	1111b	Custom

Loopback capabilities

Media side input loopback and Host side input loopback feature are supported, loopback control method refers to CMIS.

Byte	Bits	Field Name	Field Description
13h:128	6	Simultaneous Host And Media Side loopbacks	0b: not supported
	5	Per Lane Media Side Loopbacks	1b: supported
	4	Per Lane Host Side Loopbacks	1b: supported
	3	Host Side Input Loopback	1b: supported
	2	Host Side Output Loopback	1b: supported
	1	Media Side Input Loopback	1b: supported
	0	Media Side Output Loopback	1b: supported

Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

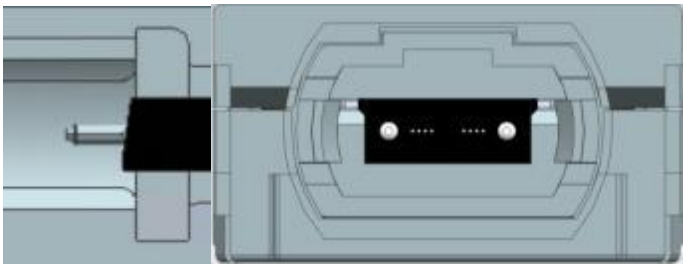
Parameter	Accuracy	Unit
Internally measured transceiver temperature1	±3	°C
Internally measured transceiver supply voltage	±3	%
Measured Tx bias current	±10	%
Measured Tx output power2	±3	dB
Measured Rx received average optical power	±3	dB

Notes:

1. Test point is the hotspot of the module.

2. DDM report stability shall be within 0.5 dB when temperature is stable. TX DDM must report -40 dBm when TX disable

Optical Interface Requirement



MPO12 APC Interface

Laser Safety

Q112-400G-SR4-01-01 are Class 1 Laser products according to FDA/CDRH, IEC-60825-1 and IEC60825-2 standards. They must be operated under the specified operating conditions

Electromagnetic Compatibility

The Q112-400G-SR4-01 are designed to meet FCC Class B limits.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	85	°C
Case Operating Temperature	Top	0	70	°C
Relative Humidity (non-condensation)	RH	15	85	%
Supply Voltage	Vcc	-0.5	3.6	V
Receiver Damage Threshold, per Lane	PRdmg	5		dBm

Operating Environments

Parameter	Symbol	Min.	Max.	Unit
Operating Case Temperature	Top	0	70	°C
Relative Humidity(non-condensing)	RH	15	85	%
Power Supply Voltage	Vcc	3.135	3.465	V
Total Power Consumption1	Pc	-	8	W
Supply Current per end			2.55	A
Bit Rate	BR		425	Gbps
Fiber Length on OM3 MMF			60	m
Fiber Length on OM4 MMF			100	m
I2C Clock Frequency	0		400	kHz

Note:

Under condition of 3.465V operating supply voltage, and 70°C case temperature.

Optical Transmitter

Parameter		Symbol	Min.	Typ.	Max.	Unit
Data Rate per Lane		DR		53.125		GBd
Modulation Format			PAM4			
Center Wavelength[1]		y	840	860	868	nm
RMS Spectral Width		σ			0.6	nm
Average Launch Power, each Lane		Pavg	-4.6		4	dBm
Optical Power OMA, each Lane, Max.		POMA	3.5			dBm
OMAouter, each Lane, Min.	max (TECQ, TDECQ) <1.8 dB		max [-2.6, max(TECQ, TECQ) – 4.4]			dBm
	1.8 < max (TECQ, TDECQ) < 4.4 dB					
Transmitter and Dispersion Eye Closure (TDECQ), each Lane		TDECQ			4.4	dB
Transmitter Eye Closure for PAM4 (TECQ), each Lane		TECQ			4.4	dB
Extinction Ratio		ER	2.5			dB
Transmitter Power Excursion, each Lane					2.3	dBm
Optical Return Loss Tolerance		ORLT			14	dB

Optical Power for TX DISABLE	-30	dBm
Encircled fluxb[2]	≥86% at 19 µm ≤30% at 4.5 µm	

Notes:

1. Defined according to the performance of the laser used.

2. Measured into type A1a.2 or type A1a.3, or A1a.4, 50 um fiber, in accordance with IEC 61280-1-

Optical Receiver

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Data Rate per Lane		BR		53.125		GBd	
Modulation Format			PAM4				
Center Wavelength		y	842	850	948	nm	
Damage Threshold			5			dBm	
Average Receive Power, each Lane			–6.4		4	dBm	
Receive Power, each Lane (OMAouter)					3.5	dBm	
Receiver Reflectance		Rr			– 15	dB	
Receiver Sensitivity, each Lane			RS = max (-4.6, TECQ – 6.4)			dBm	1
Stressed Receiver Sensitivity, each Lane					–2.0	dBm	
Rx LOS	Assert		-15			dBm	
	De-assert				-7.5	dBm	
	Hysteresis		0.5		5	dB	

Notes:

1. Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

Electrical Specification

Parameters	Min.	Typ.	Max.	Unit
Pre FEC Bit Error Ratio			2.4E-4	
Post FEC Bit Error Ratio			1E-12	
Transmitter (each Lane)				
Differential pk-pk Input Voltage Tolerance	750			mV
Differential Termination Mismatch			10	%
Eye Height	10			mV
Common-Mode to Differential-Mode Return Loss	IEEE802.3ck Equation (120G– 1)			dB
Vertical Eye Closure			12	dB
Effective Return Loss	7.3			dB
Transition Time	10			ps
Receiver (each Lane)				
Differential data output swing	300		900	mVpp
Differential Termination Mismatch			10	%
Eye Height	15			mV

Vertical Eye Closure	12	dB
Common-Mode to Differential-Mode Return Loss	IEEE802.3ck Equation (120G– 1)	
Effective Return Loss	8.5	dB
Transition Time	8.5	ps

Ordering Information

Product Name	Product Description
Q112-400G-SR4-01	400GBASE-SR4 QSFP112 PAM4 850nm MMF 100m DOM Optical Transceiver Module, MPO12 APC

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