100 Gb/s 10 km CFP2 LR4 Transceiver

CFP2 Series

- **Compliant with 100GBASE-LR4 and 4I1-9D1F**
- **Support line rates from 103.125 Gbps to 111.81 Gbps**
- **Integrated LAN WDM EML TOSA / ROSA for up to 10 km reach over SMF**
- **Digital Diagnostics Monitoring Interface**
- **Duplex LC optical receptacle**
- **No external reference clock**
- **Single 3.3 V power supply**
- **Power dissipation < 6 W**

Ascent's 100G CFP2 LR4 optical transceiver offers service providers, network operators 100 Gigabit Ethernet connectivity options for data center networking, enterprise core aggregation, and service provider transport applications. It integrates receiver and transmitter path on one module.

In the transmit side, four lanes of serial data streams are recovered, retimed, and passed to four laser drivers. The laser drivers control four EMLs (Electric-absorption Modulated Lasers) with center wavelength of 1296 nm, 1300nm, 1305nm and 1309 nm. The optical signals are multiplexed to a single-mode fiber through an industry standard LC connector.

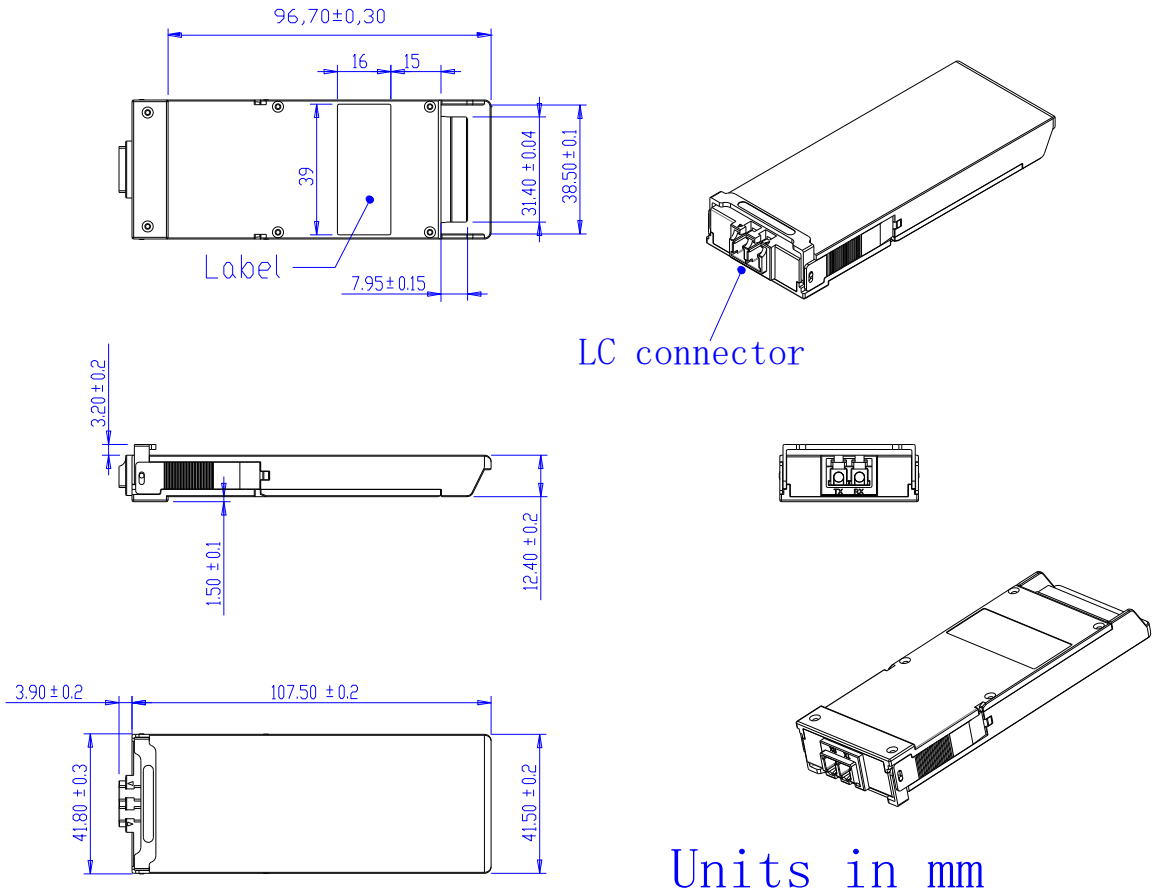
In the receive side, the four lanes of optical data streams are optically de-multiplexed by the integrated optical de-multiplexer. Each data stream is recovered by a PIN photo-detector and trans-impedance amplifier, retimed.

This module features a hot-pluggable electrical interface, low power consumption and MDIO management interface.

Key Features

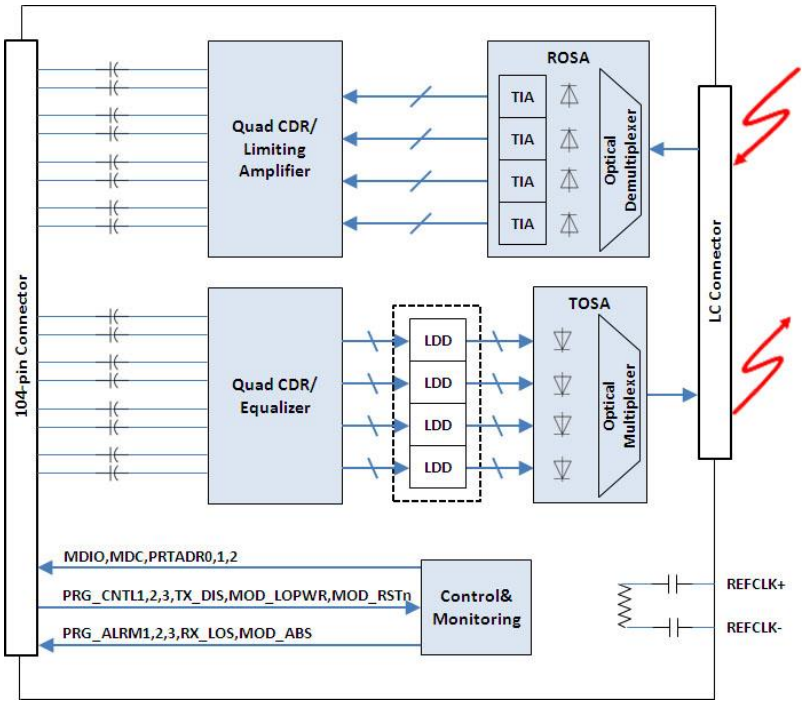
- Compliant with 100GBASE-LR4 and 4I1-9D1F
- Support line rates from 103.125 Gbps to 111.81 Gbps
- Integrated LAN WDM EML TOSA / ROSA for up to 10 km reach over SMF
- Digital Diagnostics Monitoring Interface
- Duplex LC optical receptacle
- No external reference clock
- Single 3.3 V power supply
- Case operating temperature range:0°C to 70°C
- Power dissipation < 6W

Outline Dimensions



Overview

The module provides an aggregated signaling rate from 103.125 Gbps to 111.81 Gbps. It is compliant with IEEE 802.3ba 100GBASE-LR4 and ITU-T G.959.1 4I1-9D1F , and OIF2010.404.08 CEI-28G-VSR electrical specifications. The MDIO management interface complies with IEEE 802.3ba standard. The transceiver complies with CFP MSA CFP2 Hardware Specification Rev. 1.0, CFP MSA Management Interface Specification, and OIF CEI-28G-VSR standards. A block diagram is shown in Figure 1.



CFP2 LR4 Optical Transceiver functional block diagram

Transmitter

The transmitter path converts four lanes of serial NRZ electrical data from line rate of 25.78 Gbps to 27.95 Gbps to a standard compliant optical signal. Each signal path accepts a 100 Ω differential 100 mV peak-to-peak to 900 mV peak-to-peak 25 Gbps electrical signal on TDxn and TDxp pins. Inside the module, each differential pair of electric signals is input to a CDR (clock-data recovery) chip. The recovered and retimed signals are then passed to a laser driver which transforms the small swing voltage to an output modulation that drives a EML laser. The laser drivers control four EMLs with center wavelengths of 1296 nm, 1300 nm, 1305 nm and 1309 nm. The optical signals from the four lasers are multiplexed together optically. The combined optical signals are coupled to single-mode optical fiber through an industry standard LC optical connector.

Receiver

The receiver takes incoming combined four lanes optical data from line rate of 25.78 Gbps to 27.95 Gbps through an industry standard LC optical connector. The four incoming wavelengths are separated by an optical de-multiplexer into four separated channels. Each output is coupled to a PIN photo-detector. The

electrical currents from each PIN photo-detector are converted to a voltage with a high-gain transimpedance amplifier. The electrical output is recovered and retimed by the CDR chip. The four lanes of reshaped electrical signals are output to RDxp and RDxn pins.

Low Speed Signaling

Low speed signaling is based on low voltage CMOS (LVCMOS) operating at a nominal voltage of 3.3 V for the control and alarm signals, and at a nominal voltage of 1.2 V for MDIO address, clock and data signals. All low speed inputs and outputs are based on the CFP MSA CFP2 Hardware Specification Rev. 1.0 and CFP MSA Management Interface Specification Rev. 2.2 requirements.

MDC/MDIO: Management interface clock and data lines.

PRTADR0, 1, 2: Input pins. MDIO physical port addresses.

GLB_ALEMn: Output pin. When asserted low indicates that the module has detected an alarm condition in any MDIO alarm register.

PRG_CNTL1, 2, 3: Input pins. Programmable control lines defined in the CFP MSA Management Interface Specification. Pulled up with 4.7 kΩ to 10 kΩ resistors to 3.3 V inside the CFP2 module.

TX_Disable: Input pin. When asserted high or left open the transmitter output is turned off. When Tx_Dsiable is asserted low or grounded the module transmitter is operating normally. Pulled up with 4.7 kΩ to 10 kΩ resistors to 3.3 V inside the CFP2 module.

MOD_LOPWR: Input pin. When asserted high or left open the CFP2 module is in low power mode. When asserted low or grounded the module is operating normally. Pulled up with 4.7 kΩ to 10 kΩ resistors to 3.3 V inside the CFP2 module.

MOD_RSTn: Input pin. When asserted low or grounded the module is in Reset mode. When asserted high or left open the CFP2 module is operating normally after an initialization process. Pulled down with 4.7 kΩ to 10 kΩ resistors to ground inside the CFP2 module.

PRG_ALRM1, 2, 3: Output pins. Programmable alarm lines defined in the CFP MSA Management Interface Specification.

Mod_ABS: Output pin. Asserted high when the CFP2 module is absent and is pulled low when the CFP2 module is inserted.

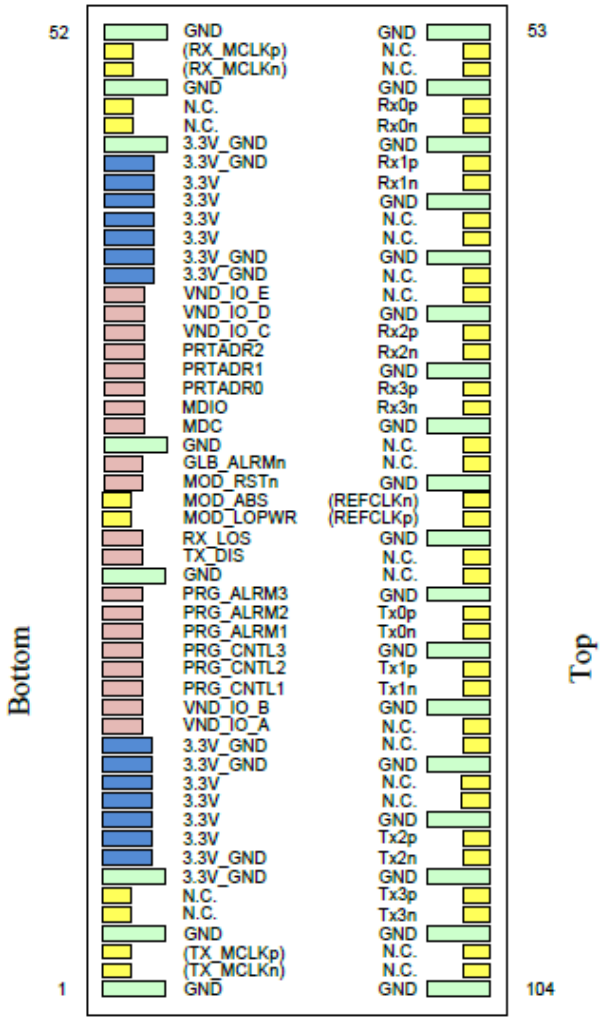
RX_LOS: Output pin. Asserted high when insufficient optical power for reliable signal reception is received.

MDIO Management Interface

The ASCENT CFP2 Optical Transceiver incorporates MDIO management interface which is used for serial ID, digital diagnostics, and certain control and status report functions. The CFP2 transceiver supports MDIO pages 8000h NVR 1 Based ID registers, 8080h NVR 2 Extended ID registers, 8100h NVR 3 network lane specific registers, and pages A000h CFP module VR 1 registers, A080h MLG VR 1 registers, A200h network lane VR 1 registers, A280h network lane VR 2 registers.

Details of the protocol and interface are explicitly described in CFP MSA Management Interface Specification. Please refer to the specifications for design reference.

Pin Assignment



CFP2 optical transceiver pin-out

CFP2 optical transceiver pin descriptions

Pin no.	Type	Name	Description
1		GND	Module ground
2	CML	(TX_MCLKn)	No connect
3	CML	(TX_MCLKp)	No connect
4		GND	Module ground
5		N.C.	No connect
6		N.C.	No connect
7		3.3V_GND	3.3V ground; tied with module ground
8		3.3V_GND	3.3V ground; tied with module ground
9		3.3V	3.3V module supply voltage
10		3.3V	3.3V module supply voltage
11		3.3V	3.3V module supply voltage

Pin no.	Type	Name	Description
12		3.3V	3.3V module supply voltage
13		3.3V_GND	3.3V ground; tied with module ground
14		3.3V_GND	3.3V ground; tied with module ground
15		VND_IO_A	Module vendor IO A; do not connect
16		VND_IO_B	Module vendor IO B; do not connect
17	LVCMOS1	PRG_CNTL1	Programmable control 1; MSA default: TRXIC_RSTn; “0”: reset; “1” or NC: not used
18	LVCMOS1	PRG_CNTL2	Programmable control 2; MSA default: Hardware interlock LSB; Default “0”: ≤ 9 W
19	LVCMOS1	PRG_CNTL3	Programmable control 3: MSA default: Hardware interlock MSB; Default “1”: ≤ 9 W
20	LVCMOS	PRG_ALRM1	Programmable alarm 1; MSA default: HIPWR_ON; “1”: module power up completed, “0”: module not high powered up
21	LVCMOS	PRG_ALRM2	Programmable alarm 2; MSA default: MOD_READY, “1”: Ready, “0”: not Ready
22	LVCMOS	PRG_ALRM3	Programmable alarm 3; MSA default:: MOD_FAULT, “1”: Fault, “0”: no Fault
23		GND	Module ground
24	LVCMOS1	TX_DIS	Transmitter disable for all lanes; “1” or NC: transmitter disabled; “0”: transmitter enabled
25	LVCMOS	RX_LOS	Receiver loss of optical signal; “1”: low optical signal, “0”: normal condition
26	LVCMOS1	MOD_LOPWR	Module low power mode; “1” or NC: module in low power mode, “0”: power on enabled
27	GND	MOD_ABS	Module absent; “1” or NC: module absent; “0”: module present. Pull up resistor on host.
28	LVCMOS2	MOD_RSTn	Module reset; “0”: reset the module; “1” or NC: module enabled
29	LVCMOS	GLB_ALRMn	Global alarm; “0”: alarm in any MDIO alarm register; “1”: no alarm condition. Pull up resistor on host.
30		GND	Module ground
31	1.2V CMOS	MDC	Management interface clock input
32	1.2V CMOS	MDIO	Management interface bi-directional data
33	1.2V CMOS	PRTADR0	MDIO physical port address bit 0
34	1.2V CMOS	PRTADR1	MDIO physical port address bit 1
35	1.2V CMOS	PRTADR2	MDIO physical port address bit 2
36		VND_IO_C	Module vendor IO C; do not connect
37		VND_IO_D	Module vendor IO D; do not connect
38		VND_IO_E	Module vendor IO E; do not connect
39		3.3V_GND	3.3V ground; tied with module ground
40		3.3V_GND	3.3V ground; tied with module ground
41		3.3V	3.3V module supply voltage
42		3.3V	3.3V module supply voltage
43		3.3V	3.3V module supply voltage

Pin no.	Type	Name	Description
44		3.3V	3.3V module supply voltage
45		3.3V_GND	3.3V ground; tied with module ground
46		3.3V_GND	3.3V ground; tied with module ground
47		N.C.	No connect
48		N.C.	No connect
49		GND	Module ground
50	CML	(RX_MCLKn)	No connect
51	CML	(RX_MCLKp)	No connect
52		GND	Module ground
53		GND	Module ground
54		N.C.	No connect
55		N.C.	No connect
56		GND	Module ground
57		RX0P	25 Gbps receiver data; Lane 0
58		RX0n	25 Gbps receiver data bar; Lane 0
59		GND	Module ground
60		RX1p	25 Gbps receiver data; Lane 1
61		RX1n	25 Gbps receiver data bar; Lane 1
62		GND	Module ground
63		N.C.	No connect
64		N.C.	No connect
65		GND	Module ground
66		N.C.	No connect
67		N.C.	No connect
68		GND	Module ground
69		RX2p	25 Gbps receiver data; Lane 2
70		RX2n	25 Gbps receiver data bar; Lane 2
71		GND	Module ground
72		RX3p	25 Gbps receiver data; Lane 3
73		RX3n	25 Gbps receiver data bar; Lane 3
74		GND	Module ground
75		N.C.	No connect
76		N.C.	No connect
77		GND	Module ground
78	CML	(REFCLKp)	Module reference clock. No connect.
79	CML	(REFCLKn)	Module reference clock. No connect.
80		GND	Module ground
81		N.C.	No connect
82		N.C.	No connect
83		GND	Module ground
84		TX0p	25 Gbps transmitter data; Lane 0
85		TX0n	25 Gbps transmitter data bar; Lane 0
86		GND	Module ground

Pin no.	Type	Name	Description
87		TX1p	25 Gbps transmitter data; Lane 1
88		TX1n	25 Gbps transmitter data bar; Lane 1
89		GND	Module ground
90		N.C.	No connect
91		N.C.	No connect
92		GND	Module ground
93		N.C.	No connect
94		N.C.	No connect
95		GND	Module ground
96		TX2p	25 Gbps transmitter data; Lane 2
97		TX2n	25 Gbps transmitter data bar; Lane 2
98		GND	Module ground
99		TX3p	25 Gbps transmitter data; Lane 3
100		TX3n	25 Gbps transmitter data bar; Lane 3
101		GND	Module ground
102		N.C.	No connect
103		N.C.	No connect
104		GND	Module ground

Notes:

1. Pulled up with 4.7 kΩ – 10 kΩ to 3.3 V inside the module.
2. Pulled down with 4.7 kΩ – 10 kΩ to GND inside the module

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	Ts	-40	-	85	°C	
Relative Humidity	RH	5	-	95	%	
Power Supply Voltage	VCC	-0.3	-	4	V	
Signal Input Voltage		Vcc-0.3	-	Vcc+0.3	V	
Receive Input Optical Power (Damage threshold)	Pdmg			5.0	dBm	

Low Speed Electrical Characteristics

Parameter	Symbol	Min..	Typ.	Max.	Unit	Notes
Supply Currents and Voltages						
Voltage	Vcc	3.2	3.3	3.4	V	With Respect to GND
Supply Current	Icc			1.8	A	
Power Dissipation	Pwr			6.0	W	
Power Dissipation (Low Power Mode)	Plp			2.0	W	
Low Speed Control and Sense Signals, 3.3 V LVCMOS						
Outputs Low Voltage	V_{OL}			0.2	V	I_{OH}=100 µA
Output High Voltage	V_{OH}	Vcc-0.2			V	I_{OH}=-100 µA
Input Low Voltage	V_{IL}	-0.3		0.8	V	
Input High Voltage	V_{IH}	2		Vcc3+0.3	V	
Input Leakage Current	I_{IN}	-10		10	µA	
Low Speed Control and Sense Signals, 1.2 V LVCMOS						
Outputs Low Voltage	V_{OL}	-0.3		0.2	V	
Output High Voltage	V_{OH}	1.0		1.5	V	
Output Low Current	I_{OL}	4			mA	
Output High Current	I_{OH}			-4	mA	
Input Low Voltage	V_{IL}	-0.3		0.36	V	
Input High Voltage	V_{IH}	0.84		1.5	V	
Input Leakage Current	I_{IN}	-100		100	µA	
Input Capacitance	C			10	pF	
MDC Clock Rate		0.1		4	MHz	

High Speed Electrical Specifications

Parameter	Symbol	Min.	Max.	Unit	Notes
Transmitter Electrical Input from Host					
Differential Voltage pk-pk		100	1200	mV	
Common Mode Noise (rms)			17.5	mV	
Differential Termination Mismatch			10	%	
Transition Time		10		ps	20/80 %
Common Mode Voltage		-0.3	2.8	V	

Eye Width	EW15	0.46		UI	At10-15probability
Eye Height	EH15	100		mV	At 10-15 probability
Receiver Electrical Output to Host					
Differential Voltage pk-pk		100	1200	mV	
Common Mode Noise (rms)			17.5	mV	
Differential Termination Mismatch			10	%	
Transition Time		9.5		ps	20/80 %
Vertical Eye Closure	VEC		6.5	dB	
Eye Width	EW15	0.57		UI	At 10-15 probability
Eye Height	EH15	240		mV	At 10-15 probability

Optical Characteristics

Specifications for 100Gbase-LR4

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Notes**
Transmitter						
Signaling Speed per Lane			25.78125 ± 100 ppm		Gbps	
Wavelength Assignment	λ0	1294.53	1295.56	1296.59	nm	
	λ1	1299.02	1300.05	1301.09	nm	
	λ2	1303.54	1304.58	1305.63	nm	
	λ3	1308.09	1309.14	1310.19	nm	
Total Output. Power	POUT			10.5	dBm	
Transmit OMA per Lane		-1.3		4.5	dBm	
Average Launch Power Per lane		-4.3		4.5	dBm	
SMSR		30			dB	
Optical Extinction Ratio	ER	4			dB	
Average launch Power off per lane	Poff			-30	dBm	
RIN	RIN			-130	dB/Hz	
Output Eye Mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}					1
Receiver						
Signaling Speed per Lane			25.78125 ± 100 ppm		Gbps	
Wavelength Assignment		1294.53	1295.56	1296.59	nm	
		1299.02	1300.05	1301.09	nm	
		1303.54	1304.58	1305.63	nm	
		1308.09	1309.14	1310.19	nm	
Receive Power (OMA) per Lane	ROMA			4.5	dBm	
Average Input Power per Channel	RXPx	-10.6		4.5	dBm	2
Receiver Sensitivity (OMA) per Lane	Rxsens			-8.6	dBm	
LOS De-Assert	LOSD	-30			dBm	
LOS Assert	LOSA			-12	dBm	
Receiver Reflectance	Rr			-26	dB	

Notes:

1. Hit ratio 5x10-5.
2. Measured with a PRBS 231-1 test pattern, @25.78Gb/s, BER<10-12 .

Specifications for OUT4 4I1-9D1F

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Signaling Speed per Lane			27.9525± 20 ppm		Gbps	
Wavelength Assignment	λ0	1294.53	1295.56	1296.59	nm	
	λ1	1299.02	1300.05	1301.09	nm	
	λ2	1303.54	1304.58	1305.63	nm	
	λ3	1308.09	1309.14	1310.19	nm	
Total Output Power	POUT			8.9	dBm	
Average Launch Power per Lane		-2.5		2.9	dBm	
SMSR		30			dB	
Optical Extinction Ratio	ER	7			dB	
Average launch Power off per Lane	Poff			-30	dBm	
Output Eye Mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}					3
Receiver						
Signaling Speed per Lane			27.9525± 20 ppm		Gbps	
Wavelength Assignment		1294.53	1295.56	1296.59	nm	
		1299.02	1300.05	1301.09	nm	
		1303.54	1304.58	1305.63	nm	
		1308.09	1309.14	1310.19	nm	
Average Input Power per Channel	RXPx	-8.8		2.9	dBm	4
Equivalent Sensitivity per Channel	Rxsens			-10.3	dBm	
LOS De-Assert	LOSD	-30			dBm	
LOS Assert	LOSA			-12	dBm	
Receiver Reflectance	Rr			-26	dB	

Notes:

1. Hit ratio $5x10^{-5}$
2. Measured with a PRBS 2^{31}-1 test pattern, @27.95Gb/s, BER<10^{-12}

Ordering Information

Product Name	Product Description
CFP2-LP-31-10	CFP2 Plug-in, CFP2-100G-LR4 Compatible 100GBASE-LR4 1296 nm, 1300nm, 1305nm and 1309nm 10km Transceiver Module, LC, DOM

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