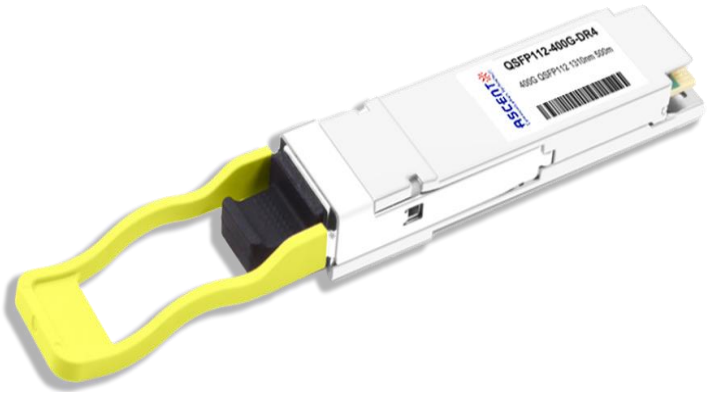
400G QSFP112 DR4 1310 nm Transceiver 500m

QSFP112 Series



- **QSFP112 MSA Compliant**
- **CMIS compliance**
- **Optical Interface: IEEE 802.3cu compliant**
- **Electrical Interface: IEEE 802.3ck 400GAUI-4**
- **Support 425Gb/s aggregate bit rate**
- **4 Parallel optical lanes**
- **MPO-12 connector**
- **Up to 500m transmission on SMF with KP4 FEC**
- **Operating temperature 0 to 70°C**

Ascent's 400 Gbps QSFP112 DR4 transceiver is a 400Gb/s Quad Small Form-factor Pluggable (QSFP) optical module design for 500 m optical communication applications. The module converts 4 input channels of 100Gb/s electrical data to 4 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 400Gb/s. Reversely, on the receiver side, the module converts 4 channels of parallel optical signals of 100Gb/s, each channel for an aggregate data rate of 400Gb/s into 4 channels of 100Gb/s electrical output data.

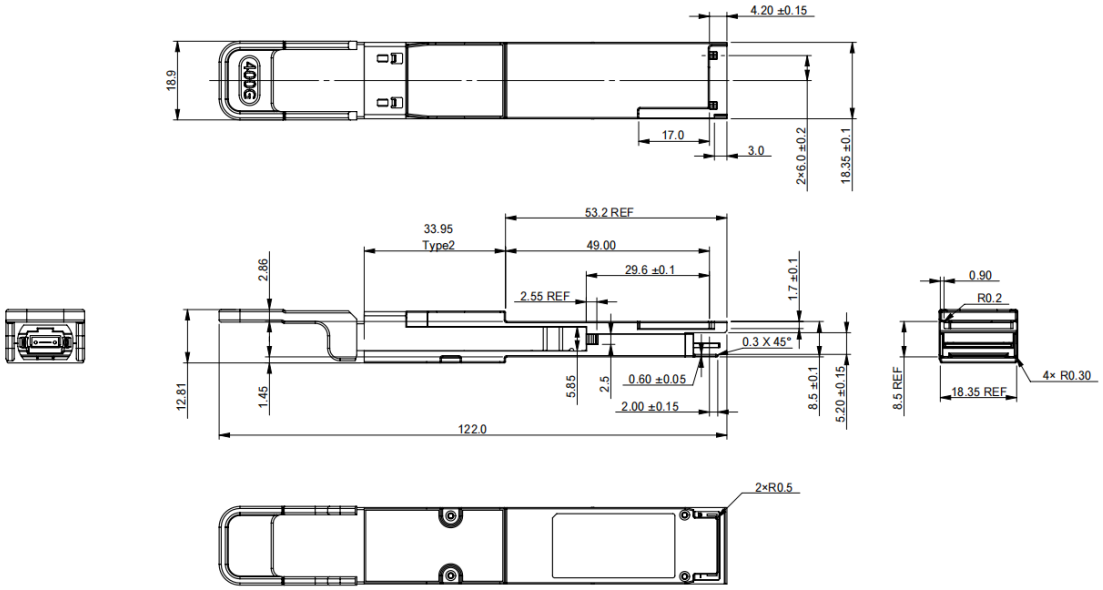
An optical fiber cable with an MTP/MPO-12 connector can be plugged into the QSFP112 DR4 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through a QSFP112 MSA-compliant edge type connector.

This product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP112 MSA Type2. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. I2C interface is supported to read and control the status of this product.

Key Features

- QSFP112 MSA Compliant
- CMIS compliance
- Optical Interface: IEEE 802.3cu compliant
- Electrical Interface: IEEE 802.3ck 400GAUI-4
- Support 425Gb/s aggregate bit rate
- 4 Parallel optical lanes
- MPO-12 connector
- Up to 500m transmission on SMF with KP4 FEC
- Operating case temperature 0 to 70°C

Outline Diagram



Pin Definitions

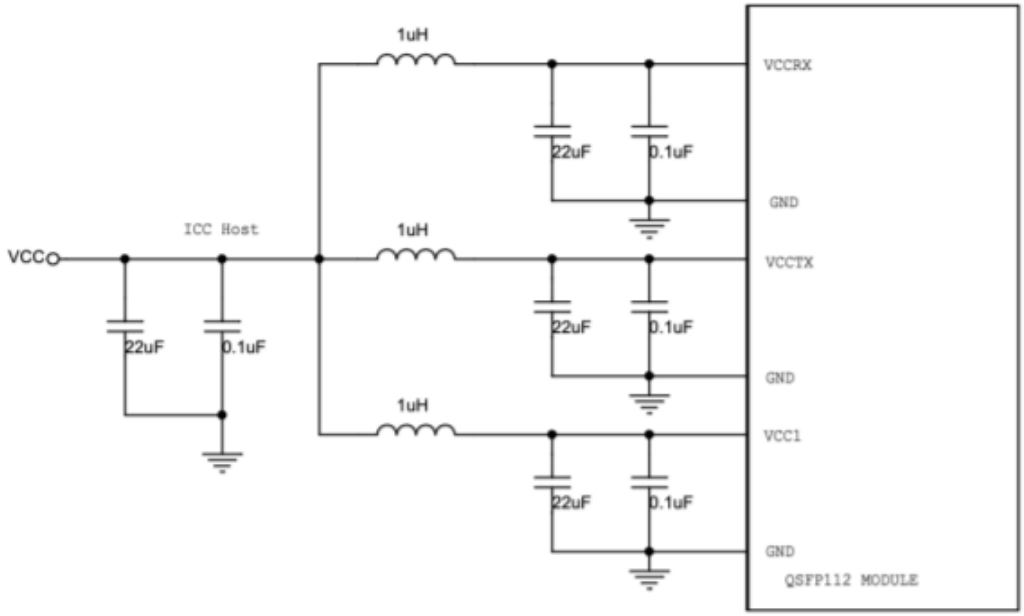
The electrical interface of QSFP112 module consist of a 38 contacts edge connector as illustrated by the diagram in below picture, which defined in Clause 4.1 of QSFP112 MSA Specification.

Pin#	Symbol	Description	Logic	Plug Sequence
1	GND		Ground	1
2	TX2n	Transmitter Data Inverted Input	CML-I	3
3	TX2p	Transmitter Data Non-Inverted Input	CML-I	3
4	GND		Ground	1
5	TX4n	Transmitter Data Inverted Input	CML-I	3
6	TX4p	Transmitter Data Non-Inverted Input	CML-I	3
7	GND		Ground	1
8	ModSelL	Module Select	LVTTL-I	3
9	ResetL	Module Reset	LVTTL-I	3
10	VccRx	+3.3V Power supply receiver		2
11	SCL	2-wire Serial interface clock	LVCMOS-I/O	3
12	SDA	2-wire Serial interface data	LVCMOS-I/O	3
13	GND		Ground	1
14	RX3p	Receiver Data Non-Inverted Output	CML-O	3
15	RX3n	Receiver Data Inverted Output	CML-O	3
16	GND		Ground	1
17	RX1p	Receiver Data Non-Inverted Output	CML-O	3
18	RX1n	Receiver Data Inverted Output	CML-O	3
19	GND		Ground	1
20	GND		Ground	1
21	RX2n	Receiver Data Inverted Output	CML-O	3
22	RX2p	Receiver Data Non-Inverted Output	CML-O	3
23	GND		Ground	1
24	RX4n	Receiver Data Inverted Output	CML-O	3

25	RX4p	Receiver Data Non-Inverted Output	CML-O	3
26	GND		Ground	1
27	ModPrsl	Module Present	LVTTL-O	3
28	IntL/RxLOS	Interrupt/optional RxLOS	LVTTL-O	3
29	VccTx	+3.3V Power supply transmitter		2
30	Vcc1	+3.3V Power Supply		2
31	LPMode/TxDis	Lower Power Mode/optional TX Disable	LVTTL-I	3
32	GND		Ground	1
33	TX3p	Transmitter Data Non-Inverted Input	CML-I	3
34	TX3n	Transmitter Data Inverted Input	CML-I	3
35	GND		Ground	1
36	TX1p	Transmitter Data Non-Inverted Input	CML-I	3
37	TX1n	Transmitter Data Inverted Input	CML-I	3
38	GND		Ground	1

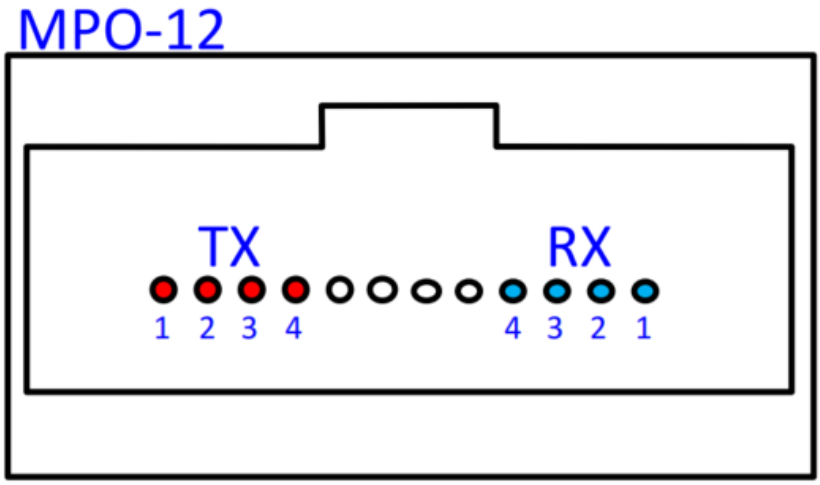
QSFP112 Control Pins

Name	Direction	Description
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host
SDA	BiDir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
IntL/RxLOS	Output	Active low IntL output port only.
LPMode/TxDis	Input	Active high LPMode input port only.



Optical Port Description

The optical interface port is a MPO-12 receptacle. The transmit and receive optical lanes shall occupy the positions depicted in below picture when looking into the MDI receptacle with the connector keyway feature on top.



ESD

This transceiver is specified as ESD threshold 1kV for high-speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser safety

This is a Class I Laser Product, or Class 1 Laser Product according to IEC/EN 60825-1:2014.
This product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.
Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	85	°C
Case Operating Temperature	Top	0	70	°C
Power Supply Voltage	Vcc	-0.5	3.6	V
Relative Humidity (non-condensation)	RH	0	85	dBm

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
Operating Case Temperature	Top	0	70	°C
Power Supply Voltage	RH	15	85	%
Data Rate, Each Lane	Vcc	3.135	3.465	V
Data Rate Accuracy	Pc	-	8	W
Pre-FEC Bit Error Ratio			2.55	A
Post-FEC Bit Error Ratio	BR		425	Gbps
Link Distance			60	m

Note:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				9.5	W	
Supply Current	Icc			2.87	A	
Module Input (each Lane)						
Signaling Rate, Each Lane	TP1	53.125 ± 100 ppm			GBd	
DC Common-Mode Input Voltage	TP1	-0.35		2.85		
Single-Ended Input Voltage	TP1a	-0.4		3.3		
AC Common-Mode Voltage Tolerance Low-Frequency, VCMLF Full-Band, VCMLF	TP1a	32 80				
Module Stressed Input Test		IEEE 802.3ck 120G3.4.3				
Differential Peak-to-Peak Input Voltage Tolerance	TP1a	750				
Common to Different Mode Input Return Loss	TP1	IEEE802.3ck Equation 120G-2				
Effective Input Return Loss	TP1	8.5				
Differential Input Termination Mismatch	TP1			10	%	
Module Output (each Lane)						
Signaling Rate, Each Lane	TP4	53.125 ± 100 ppm			GBd	
Differential Peak-to-Peak						

Output Voltage Short Mode	TP4		600	mV
Long Mode			845	
AC Common Mode Output Voltage, RMS Low-Frequency, VCMLF	TP4		32	mV
Full-Band, VCMLF			80	
Differential Termination Mismatch	TP4		10	%
Vertical Eye Closure, VEC	TP4		12	dB
Eye Height	TP4	15		mV
Common-Mode to	TP4	IEEE802.3ck Equation 120G-1		dB
Differential Mode Output Return Loss				
Effective Output Return Loss	TP4	8.5		dB
Output Transition Time (20% to 80%)	TP4	8.5		ps
DC Common-Mode Output Voltage	TP4	-350	2850	mV

Optical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Wavelength	λ	1304.5	1310	1317.5	nm	
Transmitter						
Data Rate, Each Lane			53.125 ± 100 ppm		GBd	
Modulation Format			PAM4			
Side-Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, Each Lane	P_{AVG}	-2.9		4	dBm	
Outer Optical Modulation Amplitude (OMA_{outer}), Each Lane	P_{OMA}	-0.8		4.2	dBm	1
Launch Power in OMA_{outer} Minus TDECQ, Each Lane		-2.2			dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), Each Lane	TDECQ			3.4	dB	
Extinction Ratio	ER	3.5			dB	
RIN21.4OMA	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	TOL			21.4	dB	
Transmitter Reflectance	R_T			-26	dB	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-15	dBm	
Receiver						
Data Rate, Each Lane			53.125 ± 100 ppm		GBd	
Modulation Format			PAM4			
Damage Threshold, Each Lane	THd	5			dBm	3
Average Receive Power, Each Lane		-5.9		4	dBm	4
Receive Power (OMAouter), each					dBm	

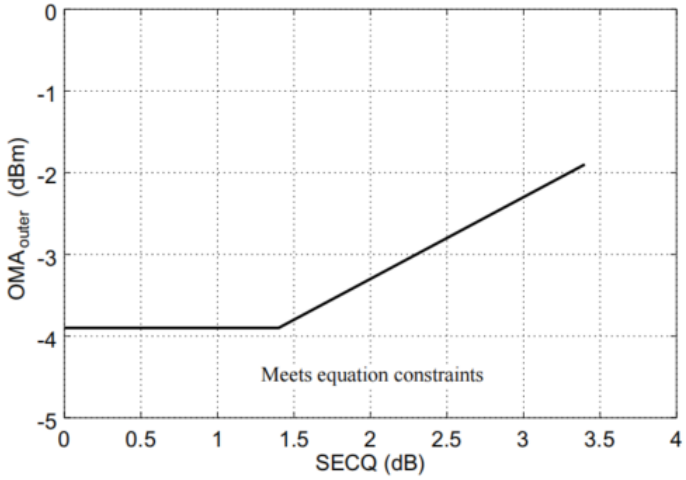
Lane			4.2		
Receiver Sensitivity (OMAouter), Each Lane	SEN		Equation (1)	dBm	5
Stressed Receiver Sensitivity (OMAouter), Each Lane	SRS		-1.9	dBm	6
Receiver Reflectance	R_R		-26	dB	
LOS Assert	LOSA	-15	-9.9		
LOS De-assert	LOSD		-6.9	dBm	
LOS Hysteresis	LOSH	0.5		dB	

Conditions of Stress Receiver Sensitivity Test (Note 7)

Stressed Eye Closure for PAM4 (SECQ), Lane under Test	3.4	dB
OMAouter of Each Aggressor Lane	4.2	dBm

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. The values for OMA_{outer} (min) vary with TDECQ. Below picture illustrates this along with the values for OMA_{outer}(max).
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity (OMA_{outer}) is informative and is defined for a transmitter with a value of SECQ up to 3.4dB. Receiver sensitivity should meet Equation (1), which is illustrated in below picture. RS = max(−3.9, SECQ – 5.3) dBm where RS is the receiver sensitivity, and TECQ is the TECQ of the transmitter used to measure the receiver sensitivity.
6. Measured with conformance test signal at TP3 for the BER equal to 2.4x10-4.
7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.



Diagnostic Characteristics

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature Monitor Absolute Error	DMI_Temp	-3	3	°C	Over operating temperature range
Supply Voltage Monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX Power Monitor Absolute Error	DMI_RX_Ch	-2	2	dB	1
Channel Bias Current Monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX Power Monitor Absolute Error	DMI_TX_Ch	-2	2	dB	1

Note:

1. Due to measurement accuracy of different single mode fibers, there could be an additional ±1 dB tolerance, or a ±3 dB total tolerance.

Ordering Information

Product Name	Product Description
Q112-400G-DR4-05	400G BASE-DR4 QSFP112 PAM4 1310nm SMF 500m DOM Optical Transceiver Module, MPO12 APC

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Specifications and product availability are subject to change without notice.

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