

400 Gb/s QSFP-DD FR4 2 km DDM Transceiver

QSFP-DD Series

- **Compliant to QSFP-DD MSA**
- **Compliant to IEEE802.3bs**
- **Compliant with 100G Lambda MSA and 400GBASE-FR4**
- **400GAUI-8 electrical interface**
- **Type 2 housing with duplex LC connector**
- **Two-wire serial interface with digital diagnostic monitoring**
- **RoHS compliant**
- **Class 1 laser**



Ascent's QSFP-DD-FR4-02 is a 400 Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) optical module designed for 2km optical communication applications. The module converts 8 channels of 50 Gb/s (PAM4) electrical input data to 4 channels of CWDM optical signals, and multiplexes them into a single channel for 400Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 400Gb/s optical input into 4 channels of CWDM optical signals, and converts them to 8 channels of 50 Gb/s (PAM4) electrical output data.

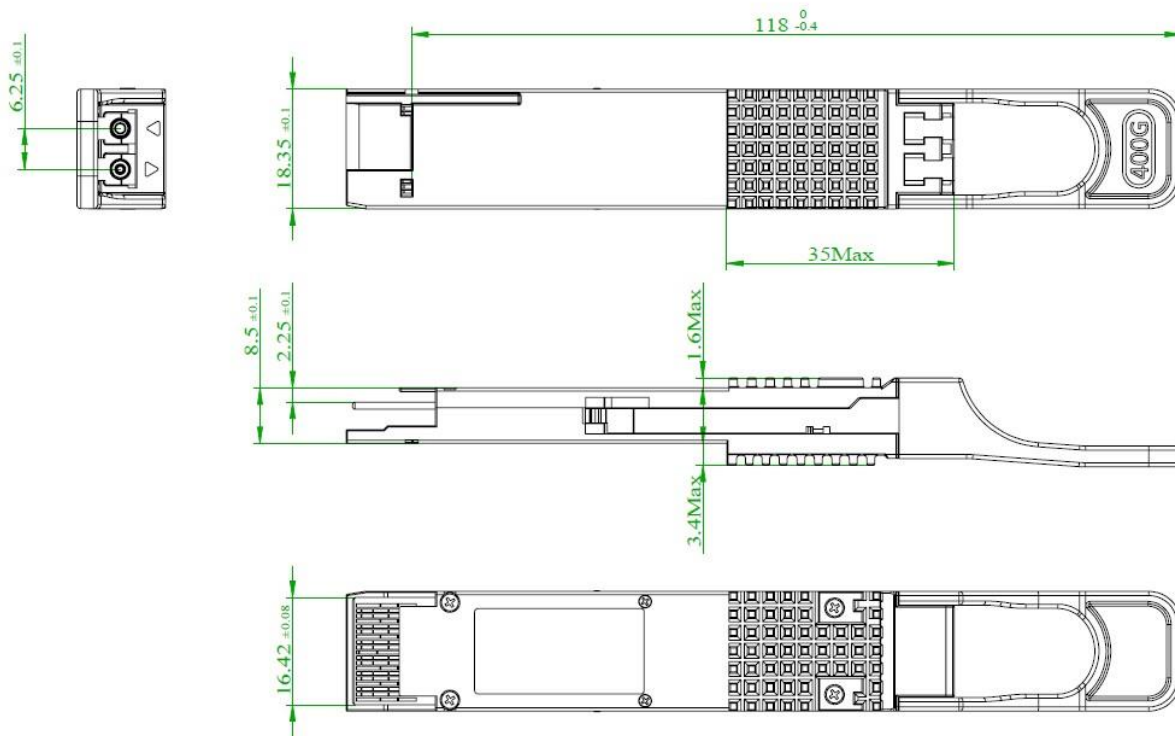
The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains a duplex LC connector for the optical interface and a 76-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module. Host FEC is required to support up to 2 km fiber transmission

QSFP-DD-FR2-02 is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Multi- Source Agreement (MSA) Type 2. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

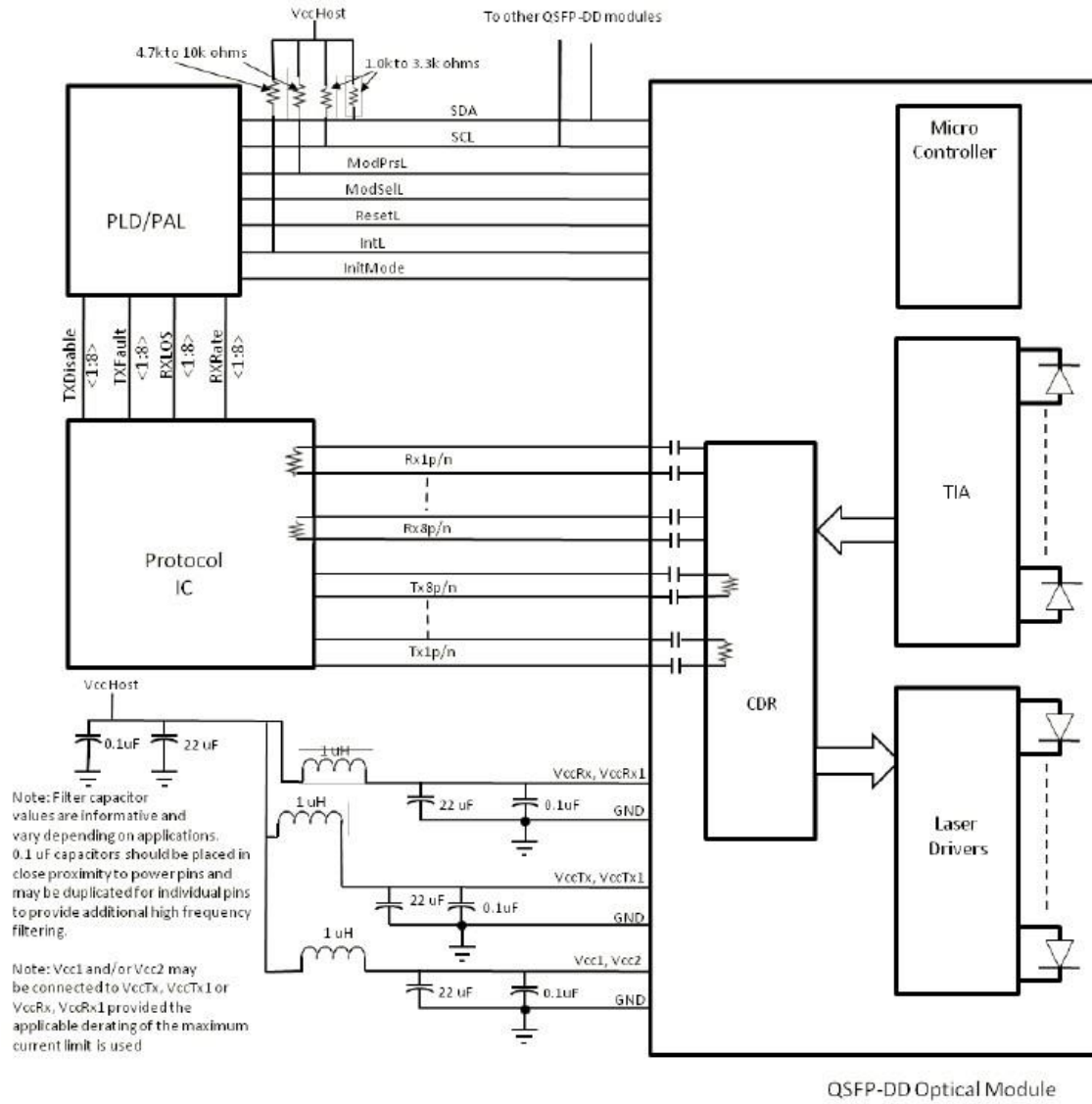
Key Features

- Compliant with 400G-FR4 Technical Specification rev 2.0 (100G Lambda MSA) and 400GBASE-FR4(IEEE802.3cu)
- Compliant with IEEE 802.3bs standard: 400GAUI-8 electrical interface
- Compliant with QSFP-DD MSA HW Rev 5.0; type 2 housing with duplex LC connector
- Compliant with QSFP-DD CMIS Rev 4.0
- Maximum power consumption 12 W
- Case operating temperature 0°C to 70°C
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1 Laser

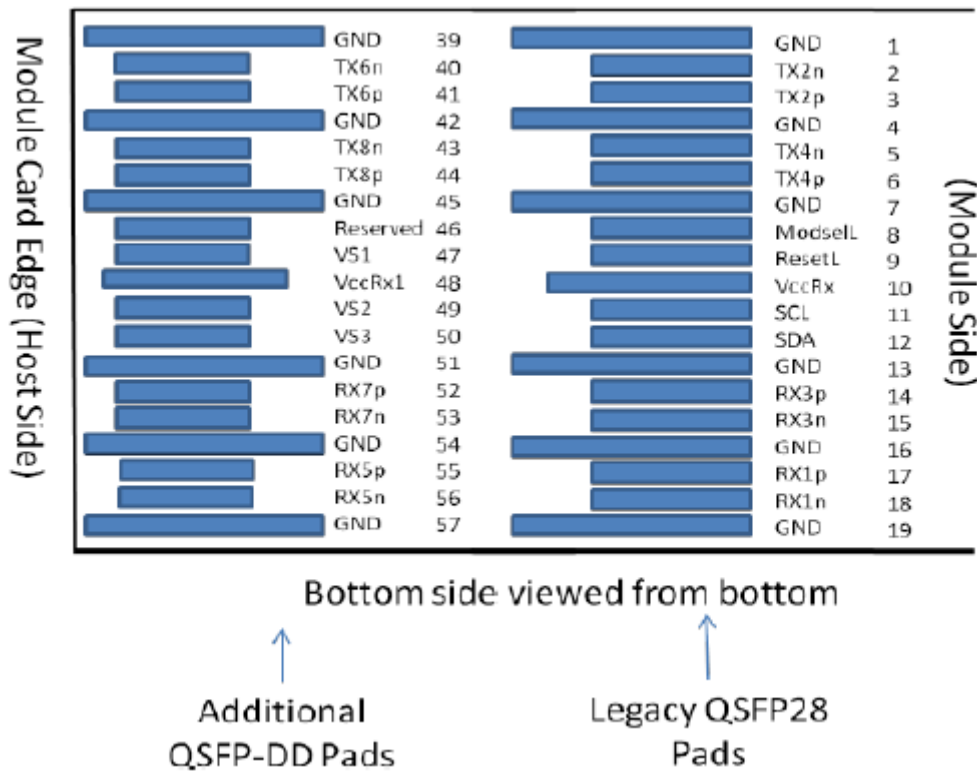
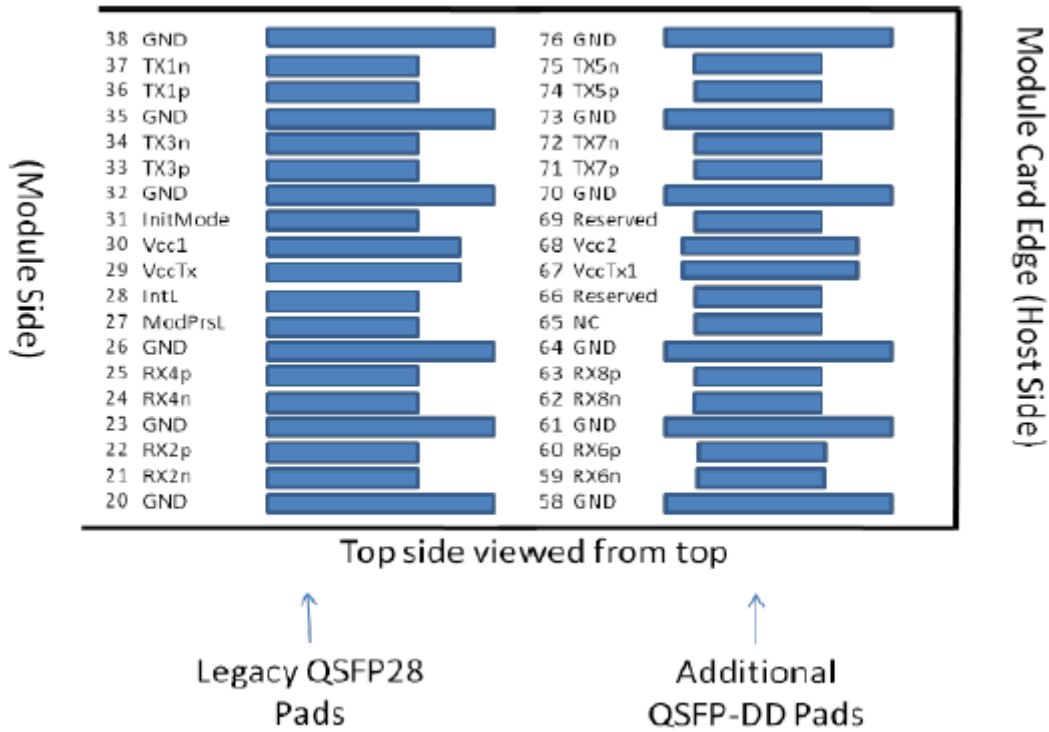
Outline Dimensions



Recommended QSFP-DD Host Board Schematic



Pin Assignment



Pin	Logic	Symbol	Definition
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		VccRx	+3.3 V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL	Interrupt
29		VccTx	+3.3 V Power Supply Transmitter
30		Vcc1	+3.3 V Power Supply
31	LVTTL-I	InitMode	Initialization Mode; in Legacy QSFP applications, the InitMode pad is called LPMODE
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	Tx6n	Transmitter Non-Inverted Data Input

41	CML-I	Tx6p	Transmitter Non-Inverted Data Output
42		GND	Ground
43	CML-I	Tx8n	Transmitter Non-Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-Inverted Data Output
45		GND	Ground
46		Reserved	For future use
47		VS1	Module Vendor Specific 1
48		VccRx1	3.3 V Power Supply
49		VS2	Module Vendor Specific 2
50		VS3	Module Vendor Specific 3
51		GND	Ground
52	CML-O	Rx7p	Receiver Non-Inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	Rx5p	Receiver Non-Inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-Inverted Data Output
61		GND	Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-Inverted Data Output
64		GND	Ground
65		NC	No Connect
66		Reserved	For future use
67		VccTx1	3.3 V Power Supply
68		Vcc2	3.3 V Power Supply
69		Reserved	For future use
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-Inverted Data Output
72	CML-I	Tx7n	Transmitter Inverted Data Output
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-Inverted Data Output
75	CML-I	Tx5n	Transmitter Inverted Data Output
76		GND	Ground

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	TS	-40	85	°C	
Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	Non-condensing
Data Input Voltage Differential	$ V_{DIP}-V_{DIN} $	-	1	V	
Control Input Voltage	VI	-0.3	$V_{CC}+0.5$	V	
Control Output Voltage	VI	-20	20	V	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Case Temperature	T _{OPR}	0	-	70	°C	
Power Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Instantaneous Peak Current at Hot Plug	I _{CC_IP}	-	-	4800	mA	
Sustained Peak Current at Hot Plug	I _{CC_SP}	-	-	3960	mA	
Maximum Power Consumption	P _D	-	-	12	W	
Maximum Power Consumption, Low Power Mode	P _{DLP}	-	-	1.5	W	
Signaling Rate per Lane	SRL	-	53.125	-	GBd	1
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise Tolerance	-	-	-	66	mV	2
Rx Differential Data Output Load	-	-	100	-	Ω	
Operating Distance	-	2	-	2000	m	

Notes:

1. PAM4
2. 10 Hz to 10 MHz

Electrical Specification High Speed Signal (compliant with IEEE 802.3bs 400GAUI-8)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Receiver (Module Output)						
AC Common-Mode Output Voltage (RMS)	-	-	-	17.5	mV	
Differential Output Voltage	-	-	-	900	mV	
Near-End Eye Height, Differential	70	-	-	-	mV	
Far-End Eye Height, Differential	30	-	-	-	mV	
Far End Pre-Cursor Ratio	-4.5	-	-	2.5	%	
Differential Termination Mismatch	-	-	-	10	%	
Transition Time (Min., 20% To 80%)	9.5	-	-	-	ps	
DC Common Mode Voltage	-350	-	-	2850	mV	
Transmitter (Module Input)						
Differential pk-pk Input Voltage Tolerance	900	-	-	-	mV	

Differential Termination Mismatch	-	-	10	%
Single-Ended Voltage Tolerance Range	-0.4	-	3.3	V
DC Common Mode Voltage	-350	-	2850	mV

Electrical Specification Low Speed Signal (compliant with QSFP-DD HW Rev 5.0)

Parameter	Symbol	Min.	Max.	Unit	Note
Module Output SCL and SDA	V _{OL}	0	0.4	V	
Module Input SCL and SDA	V _{IL}	-0.3	V _{CC} *0.3	V	
	V _{IH}	V _{CC} *0.7	V _{CC} +0.5	V	
InitMode, ResetL, and ModSelL	V _{IL}	-0.3	0.8	V	
	V _{IH}	2	V _{CC} +0.3	V	
IntL	V _{OL}	0	0.4	V	
	V _{OH}	V _{CC} -0.5	V _{CC} +0.3	V	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Transmitter						
Wavelength L0	λ _{C0}	1264.5	1271	1277.5	nm	
Wavelength L1	λ _{C1}	1284.5	1291	1297.5	nm	
Wavelength L2	λ _{C2}	1304.5	1311	1317.5	nm	
Wavelength L3	λ _{C3}	1324.5	1331	1337.5	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Average Launch Power, each Lane	AOPL	-3.3	-	3.5	dBm	1
Outer Optical Modulation Amplitude (OMA _{outer}), each Lane	T _{OMA}	-0.3	-	3.7	dBm	2
Difference in Launch Power between any Two Lanes (OMA _{outer})	DP	-	-	4	dB	
Launch Power in OMA _{outer} Minus TDECQ for ER ≥ 4.5 dB, each Lane	T _{OMA} - TDECQ	-1.7	-	-	dBm	
Launch Power in OMA _{outer} Minus TDECQ for ER <4.5 dB, each Lane	T _{OMA} - TDECQ	-1.6	-	-	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ	-	-	3.4	dB	
TDECQ - 10*log ₁₀ (Ceq), each Lane		-	-	3.4	dB	
Average Launch Power of OFF Transmitter, each Lane	T _{OFF}	-	-	-20	dBm	
Extinction Ratio, each lane	ER	3.5	-	-	dB	
Transmitter Transition Time	TT	-	-	17	ps	
RIN _{17,1OMA}	RIN	-	-	-136	dB/Hz	
Optical Return Loss Tolerance	ORL	-	-	17.1	dB	
Transmitter Reflectance	T _R	-	-	-26	dB	3
Receiver						
Wavelength L0	λ _{C0}	1264.5	1271	1277.5	nm	
Wavelength L1	λ _{C1}	1284.5	1291	1297.5	nm	

Wavelength L2	λ_{C2}	1304.5	1311	1317.5	nm	
Wavelength L3	λ_{C3}	1324.5	1331	1337.5	nm	
Damage Threshold, each Lane	AOP _D	4.5	-	-	dBm	
Average Receive Power, each Lane	AOP _R	-7.3	-	3.5	dBm	4
Receive Power (OMA _{outer}), each Lane	OMA _R	-	-	3.7	dBm	
Difference in Receive Power between any Two Lanes (OMA _{outer})	DR	-	-	4.1	dB	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver Sensitivity (OMA _{outer}), each lane	S _{OMA}	-	-	Max(-4.6, SECQ-6)	dBm	5
Stressed Receiver Sensitivity (OMA _{outer}), each lane	SRS	-	-	-2.6	dBm	6

Conditions of Stressed Receiver Sensitivity Test

Stressed Eye Closure for PAM4 (SECQ)	-	-	3.4	-	dB	
SECQ - $10 \cdot \log_{10}(C_{eq})$, Lane under Test (Max.)	-	-	-	3.4	dB	
OMA _{outer} of each Aggressor Lane	-	-	1.5	-	dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 4.5 dB or TDECQ < 1.3 dB for an extinction ratio of < 4.5 dB, the OMA_{outer} (min.) must exceed this value.
3. Transmitter reflectance is defined looking into the transmitter.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength.
5. Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.
6. Measured with conformance test signal at TP3 for the BER = 2.4×10^{-4} .

Timing for Soft Control and Status Functions

Parameter	Symbol	Min.	Max.	Unit	Notes
MgmtInit Duration		-	2000	ms	
ResetL Assert Time	t_reset_init	10	-	μ s	
IntL Assert Time	ton_IntL	-	200	ms	
IntL Deassert Time	toff_IntL	-	500	μ s	
Rx LOS Assert Time	ton_los	-	100	ms	
Rx LOS Assert Time (fast mode)	ton_losf	-	1	ms	
Tx Fault Assert Time	ton_Txfault	-	200	ms	
Flag Assert Time	ton_flag	-	200	ms	
Mask Assert Time	ton_mask	-	100	ms	
Mask Deassert Time	toff_mask	-	100	ms	

I/O Timing for Squelch and Disable

Parameter	Symbol	Min.	Max.	Unit	Notes
Rx Squelch Assert Time	ton_Rxsq	-	500	ms	
Rx Squelch Deassert Time	toff_Rxsq	-	15	s	
Tx Squelch Assert Time	ton_Txsq	-	400	ms	
Tx Squelch Deassert Time	toff_Txsq	-	5	s	
Tx Disable Assert Time	ton_Txdis	-	100	ms	
Tx Disable Assert Time (fast mode)	ton_Txdisf	-	3	ms	
Tx Disable Deassert Time	toff_Txdis	-	400	ms	
Tx Disable Deassert Time (fast mode)	toff_Txdisf	-	10	ms	
Rx Output Disable Assert Time	ton_Rxdis	-	100	ms	
Rx Output Disable Deassert Time	toff_Rxdis	-	100	ms	
Squelch Disable Assert Time	ton_sqdis	-	NA	ms	Not supported
Squelch Disable Deassert Time	toff_sqdis	-	NA	ms	Not supported

Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to VCC	3%	V	Internal
Tx Bias Current (each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (each Lane)	-3.3 to +3.5	±3	dB	Internal
Rx Receive Power (each Lane)	-7.3 to +3.5	±3	dB	Internal

Ordering Information

Product Name	Product Description
QSFP-DD-FR4-02	QSFP DD PAM4 Plug-in, 400GBASE-FR4 2km, 1271, 1291, 1311 and 1331nm Optical Transceiver, LC Duplex, DOM

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